珠海三泰克科技有限公司

San Technology (Zhuhai) Co., Ltd.

SPECIFICATION

FOR

LCD Module

Customer P/N:

Santek P/N: ST0295A1W-RSMLW-F

DOC. Revision: RS01

Customer Approval:

	SIGNATURE	DATE
PREPARED BY	Aaron Lu	2024-03-23
CHECKED BY	Andy Song	2024-3-25
APPROVED BY	Natty Lee	2024.Mar.25

Document Revision History

Version	Revise Date	Description	Changed by
RS01	2024-03-23	First issue	Aaron Lu

Table of Contents

1. General Specification

1.1 Description

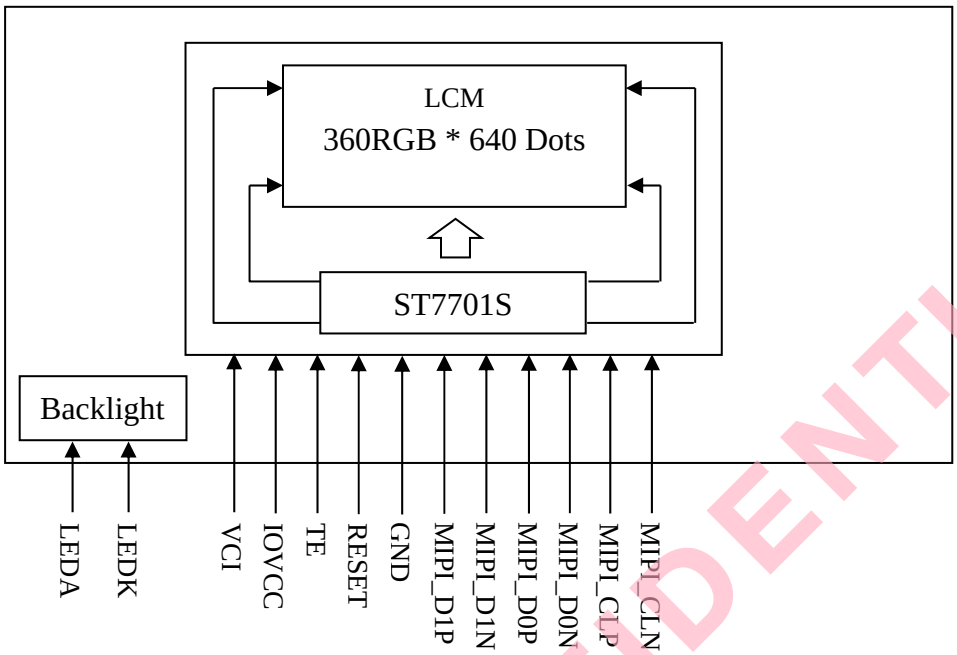
Santek Display model ST0295A1W-RSMLW-F is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 2.95 (9:16) inch diagonally measured active display area with nHD (360 horizontal by 640 vertical pixel) resolution.

1.2 General Specification

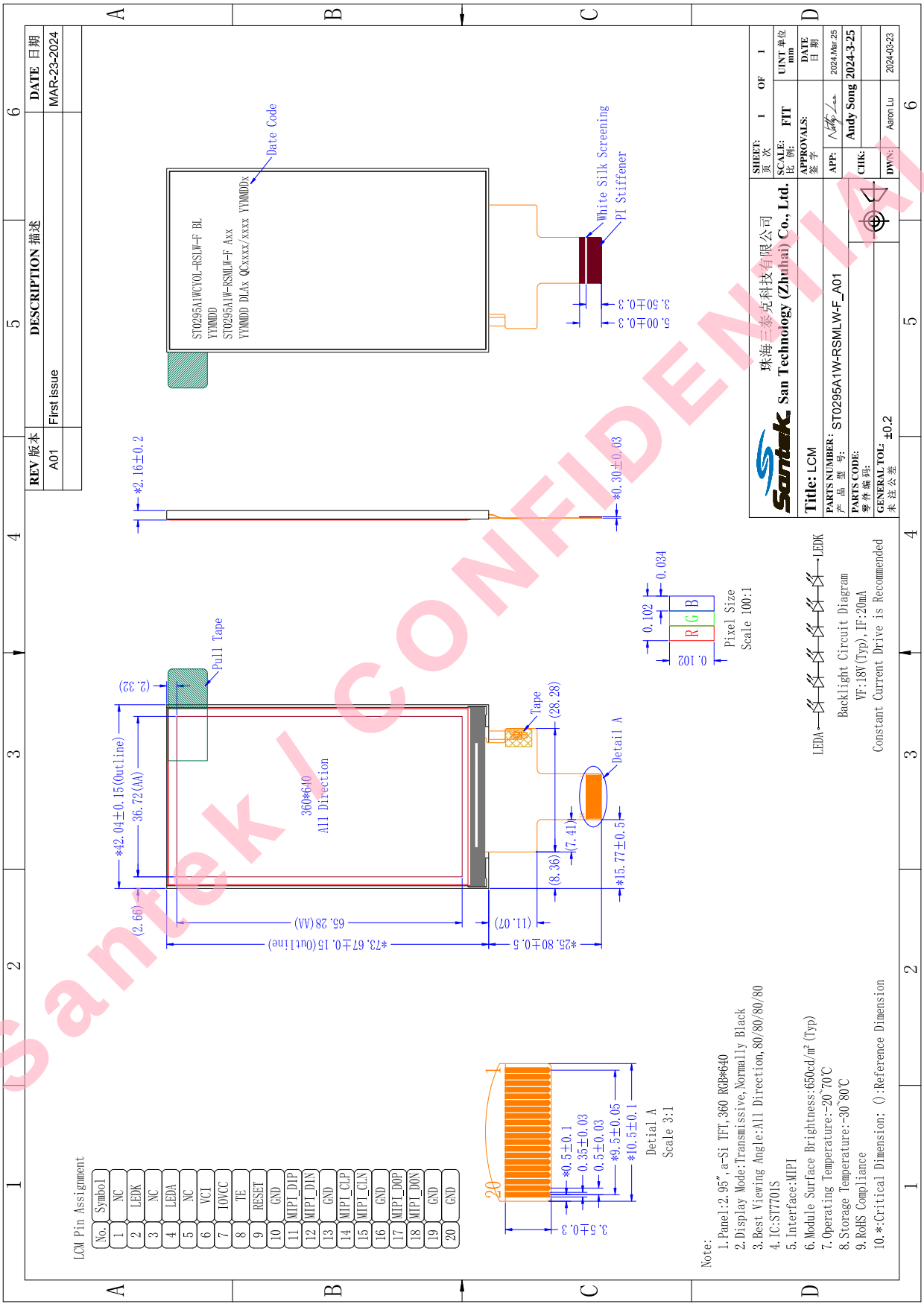
Item	Specification	Uints
LCD Type	2.95	inch
Resolution	360*640	dots
Pixel Arrangement	RGB Vertical Stripe	-
Display Mode	Normally Black, Transmissive	-
Viewing Direction	All Direction	-
Drive IC	ST7701S	-
Interface	MIPI	-
Module Size	62.80(W) x 82.80(H) x 3.79(D)	mm
Active Area	36.12(W) x 64.68(H)	mm
Pixel Pitch	0.102(W) x 0.102(H)	mm
Operating Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note: Please refer to the mechanical drawing.

2. Block Diagram



3. Mechanical Drawing



4. Pin Description

Pin	Symbol	Function Descriptions
1	NC	No connect.
2	LEDK	Power supply for backlight (Cathode).
3	NC	No connect.
4	LEDA	Power supply for backlight (Anode).
5	NC	No connect.
6	VCI	Power Supply for internal Circuit.
7	IOVCC	Power Supply for IO System.
8	TE	No connect.
9	RESET	The external reset input.
10	GND	System ground.
11	MIPI_D1P	MIPI DSI differential data pair.
12	MIPI_D1N	
13	GND	System ground.
14	MIPI_CLP	MIPI DSI differential clock pair.
15	MIPI_CLN	
16	GND	System ground.
17	MIPI_D0P	MIPI DSI differential data pair.
18	MIPI_D0N	
19	GND	System ground.
20	GND	System ground.

5. Driver Electrical Characteristics

5.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3 ~ +4.6	V
Supply Voltage(Logic)	VDDI	-0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3~VDDI+0.3	V
Logic Output Voltage Range	VO	-0.3~VDDI+0.3	V
Operating Temperature Range	TOPR	-20 ~ +70	℃
Storage Temperature Range	TSTG	-30 ~ +80	℃

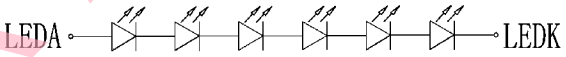
Note 1: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

5.2 Backlight Specification

Item	Symbol	Min	Typ	Max	Unit
Forward Current	I_F	-	20	-	mA
Forward Voltage	V_F	16.8	18.0	19.6	V
Backlight Power Consumption	W_{BL}	-	0.36	-	W

Note1: If LED is driven by high current, high ambient temperature & humidity condition.
The life time of LED will be reduced.

Note2: Constant current drive is recommended.



Backlight Circuit Diagram

5.3 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.5	2.8	3.6	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		11.5		17	V	
Gate Driver Low Voltage	VGL		-7.6		-12	V	
Gate Driver Supply Voltage		| VGH-VGL |	-		30	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Gamma Reference Voltage(Positive)	VAP		4.4		6.4	V	
Gamma Reference Voltage(Negative)	VAN		-2.6		-4.6	V	
Source Output Settling Time	Tr	Below with 99% precision			10	us	Note 2

Table 2 Basic DC Characteristics

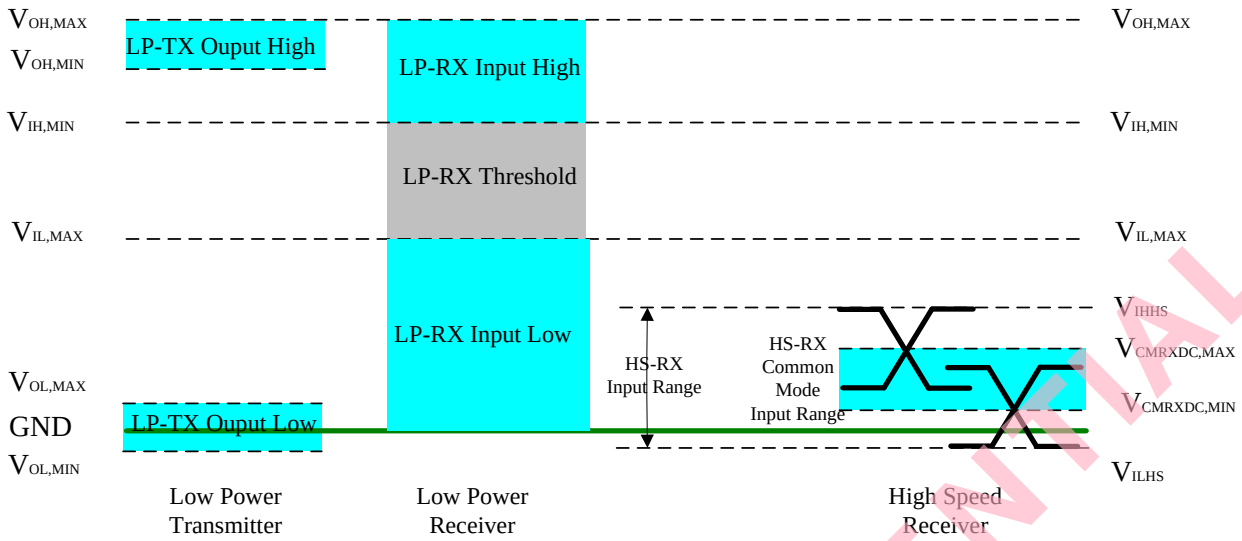
Notes:

1. Typical: VDDI=1.8V, VDD=2.8V; Ta=25 ℃

2. The Max. value is between measured point of source output and gamma setting value.

3. When evaluating the maximum and minimum of VGH, VDD=2.8V.

4. The maximum value of |VGH-VGL| can no over 30V.



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

5.4 Power Consumption

MIPI Interface

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (uA)	IDD (uA)	IDDI (uA)	IDD (uA)
Sleep-in mode	--	5	70	10	150

Notes:
1. The Current Consumption is DC characteristics of ST7701S.
2. Typical: VDDI=1.8V, VDD=2.8V;

5.5 AC Characteristics

5.5.1 MIPI Interface Characteristics

5.5.1.1 High Speed Mode

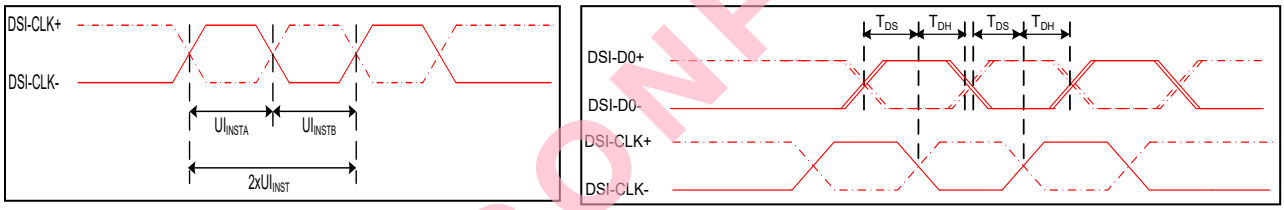


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

5.5.1.2 Lower Power Mode

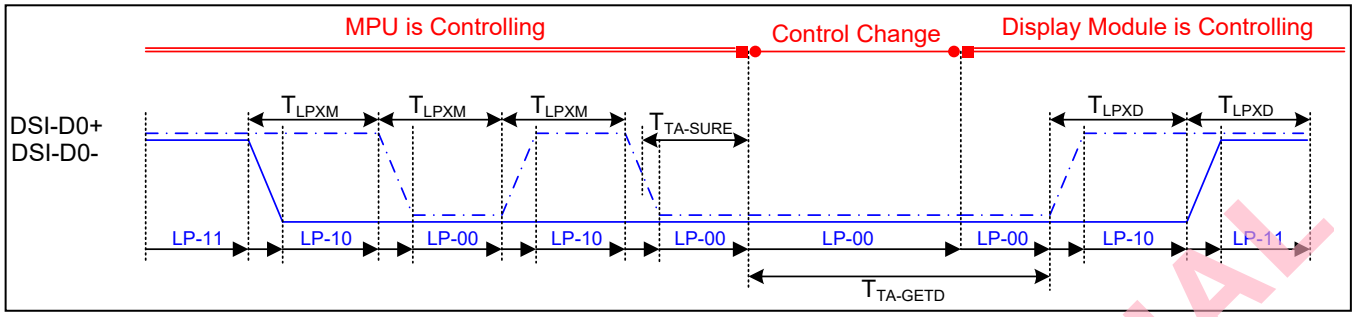


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

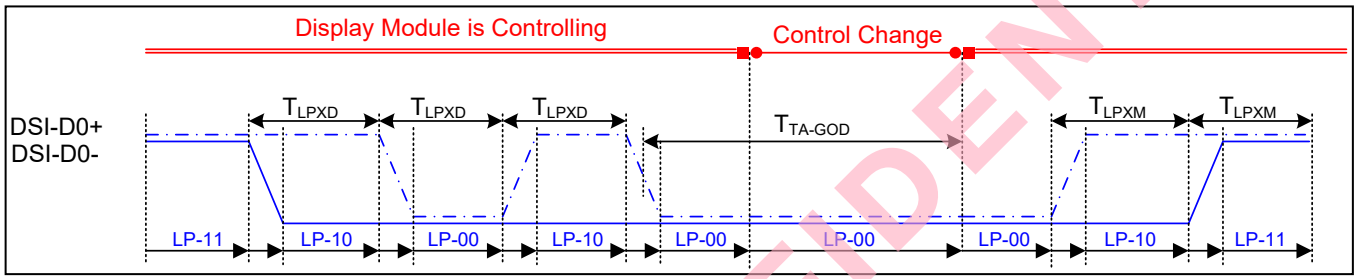


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

5.5.1.3 DSI Bursts Mode

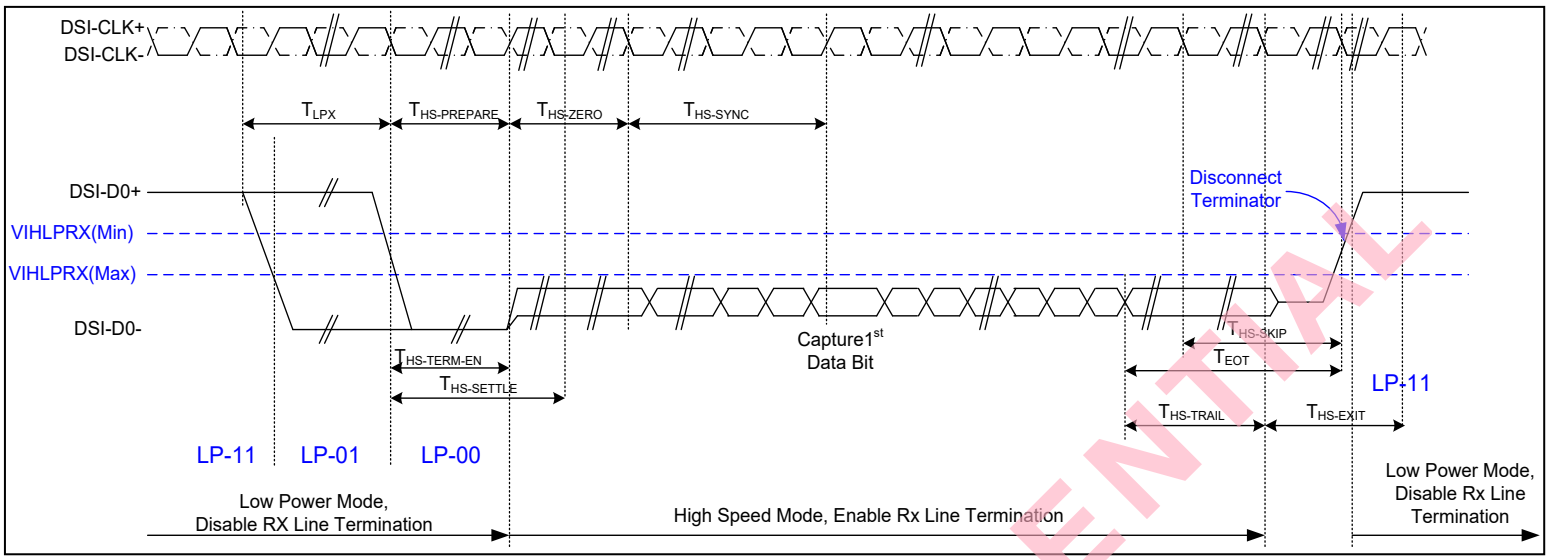


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

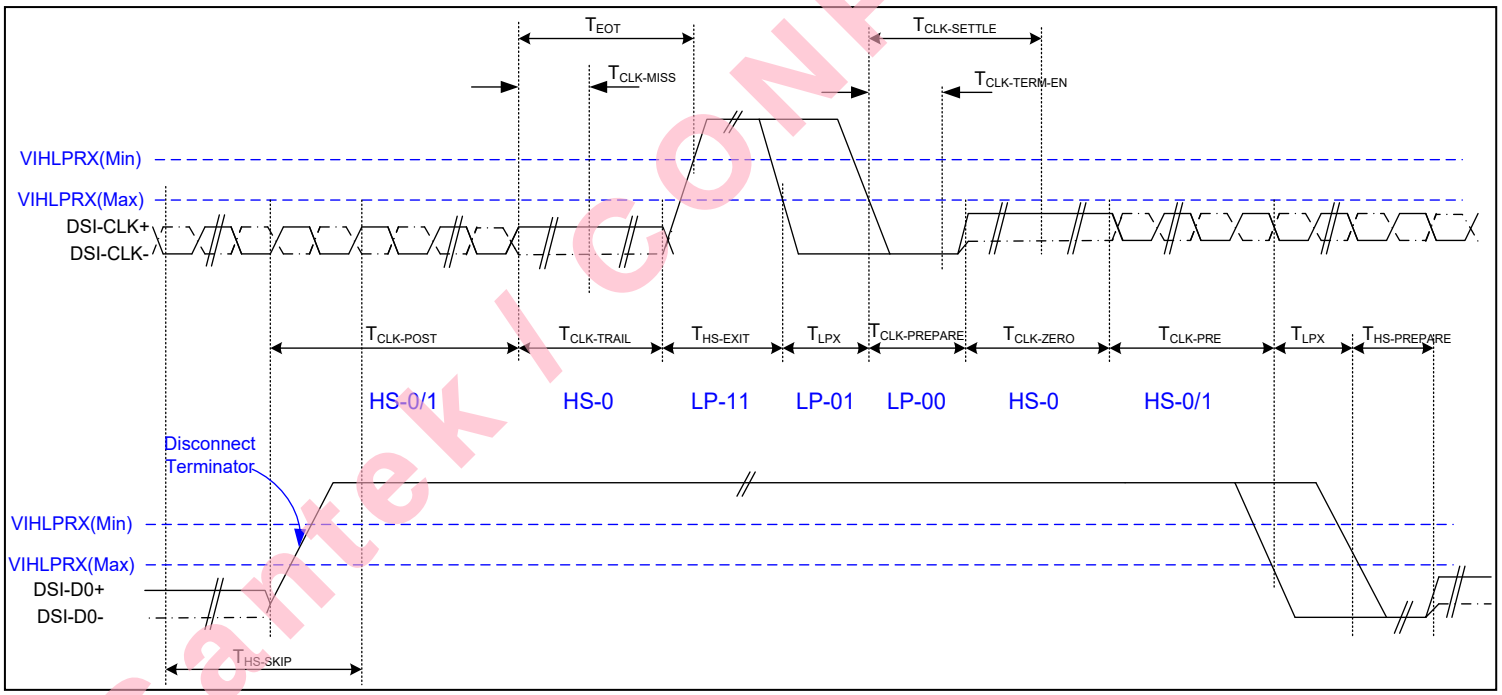


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns+12 UI	ns	Input

5.5.1.4 Reset Timing

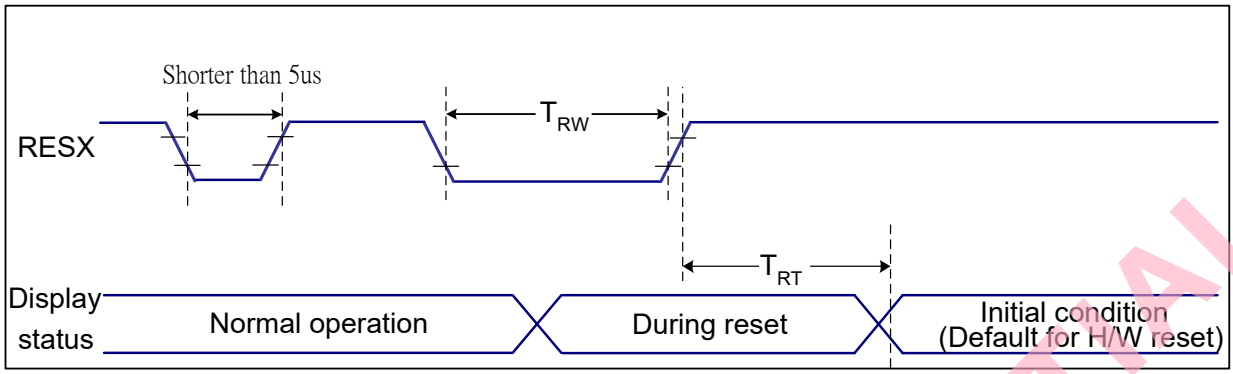


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

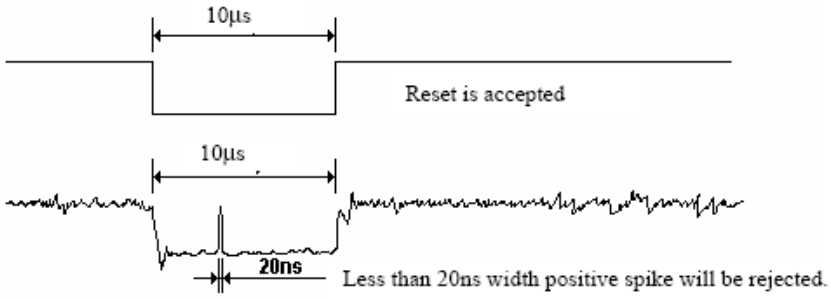
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6. Power ON/OFF Sequence

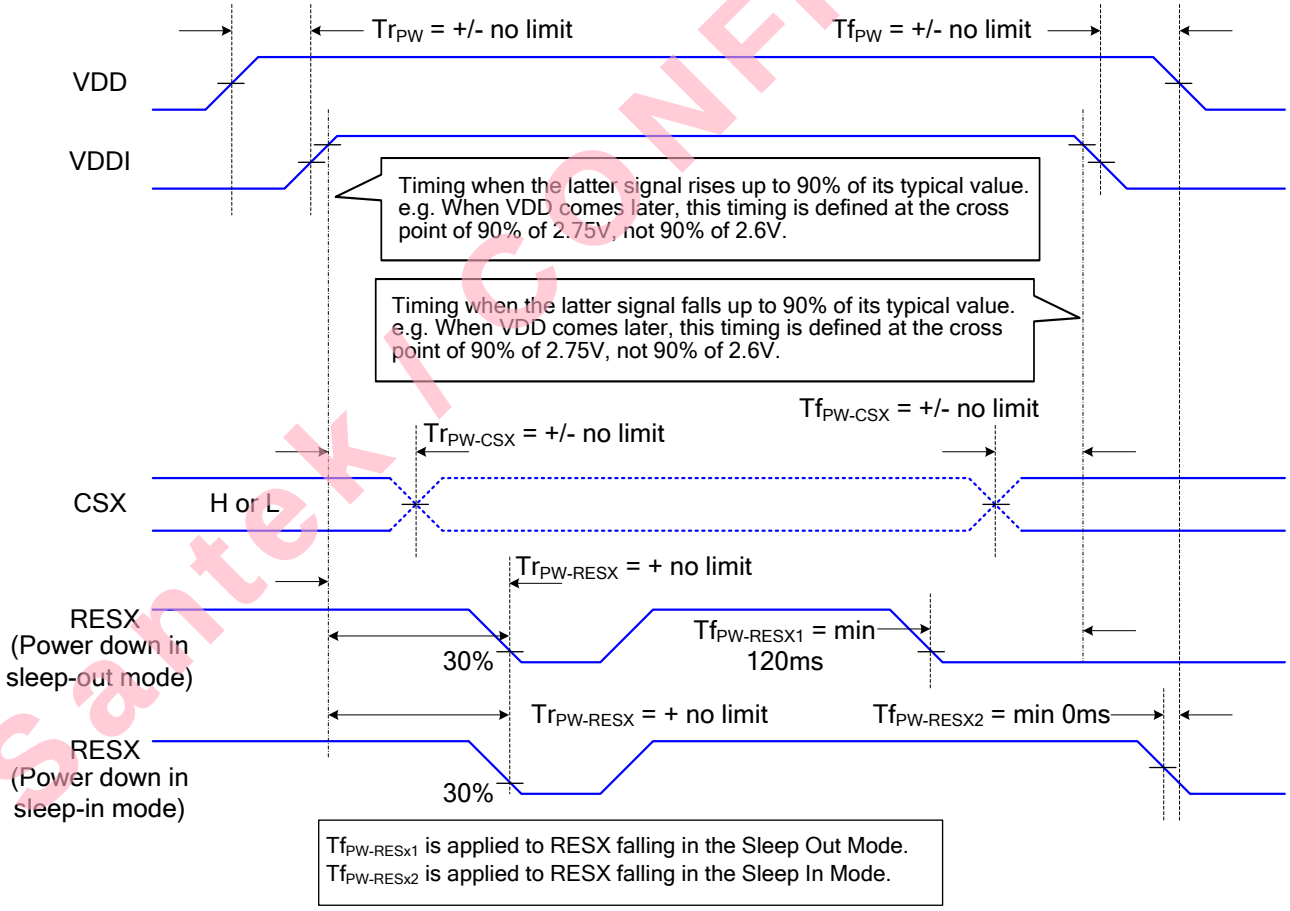
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



6.1 Uncontrolled Power Off

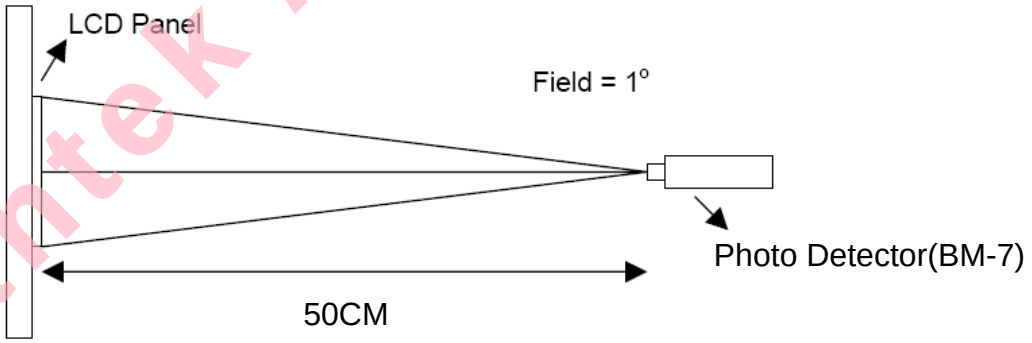
The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7. Optical Characteristics

Item		Symbol	Specifications			Unit	Note
			Min	Typ	Max		
Contrast Ratio		Cr(Θ=0°)	500	800	-	-	Note 1,2
Response Time(25℃)		Tr+Tf(Θ=0°)	-	30	45	ms	Note 3
Viewing Angle (Cr≥10)	Θ_R	ϕ=0°	-	80	-	deg	Note 4
	Θ_T	ϕ=90°	-	80	-		
	Θ_L	ϕ=180°	-	80	-		
	Θ_B	ϕ=270°	-	80	-		
Chromaticity (Θ=0°)	White	x	0.2518	0.3018	0.3518	-	Note 1,5
		y	0.2965	0.3465	0.3965		
	Red	x	0.5741	0.6241	0.6741		
		y	0.3010	0.3510	0.4010		
	Green	x	0.2713	0.3213	0.3713		
		y	0.5581	0.6081	0.6581		
	Blue	x	0.0951	0.1451	0.1951		
		y	0.0465	0.0965	0.1465		
Luminance		Θ=0°	520	650	-	cd/m^2	Note 1,6
Luminance Uniformity		-	70	85	-	%	Note 1,7
Color Gamut(NTSC)		-	-	63	-	%	Reference

Note 1: Definition of contrast ratio

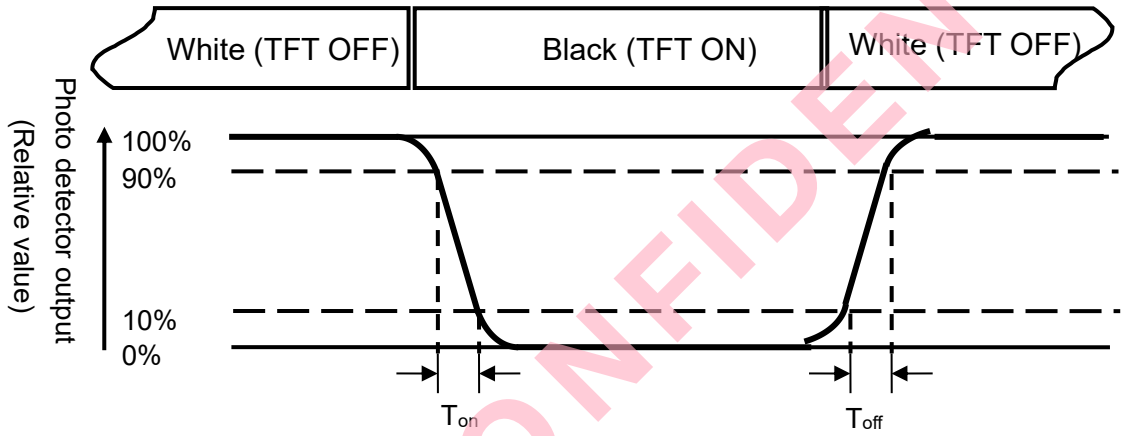


Note 2: Definition of contrast ratio

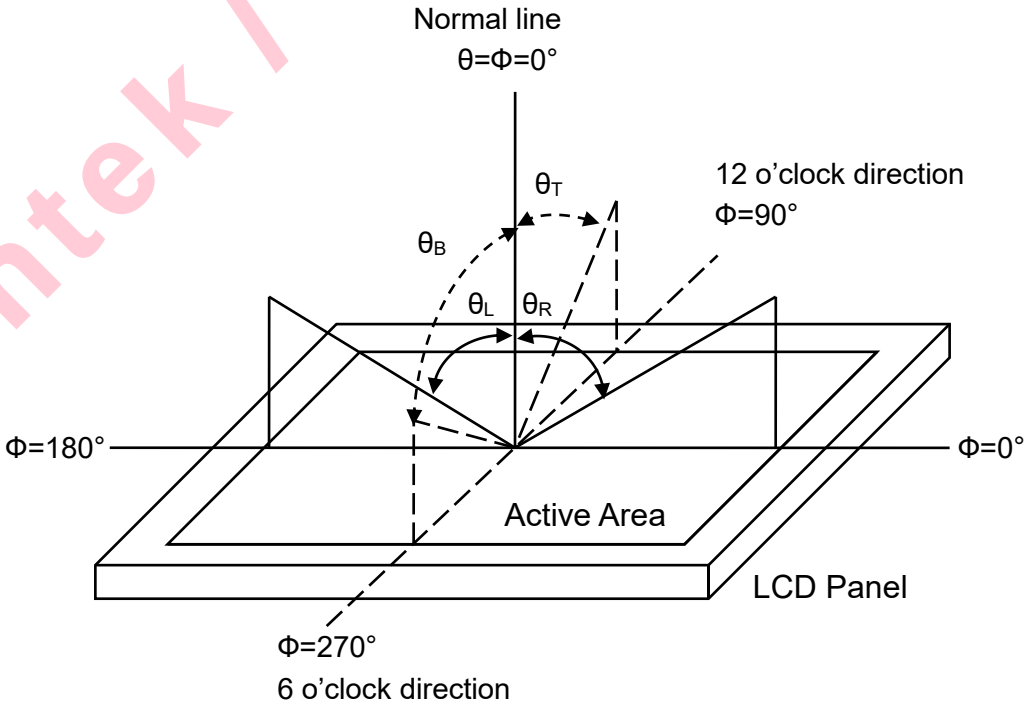
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.



Note 4: Definition of viewing angle range



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

Note 6: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 9 spot. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity } (U_L) = \frac{L_{min}}{L_{max}} \times 100\%$$

L-------Active area length W----- Active area width

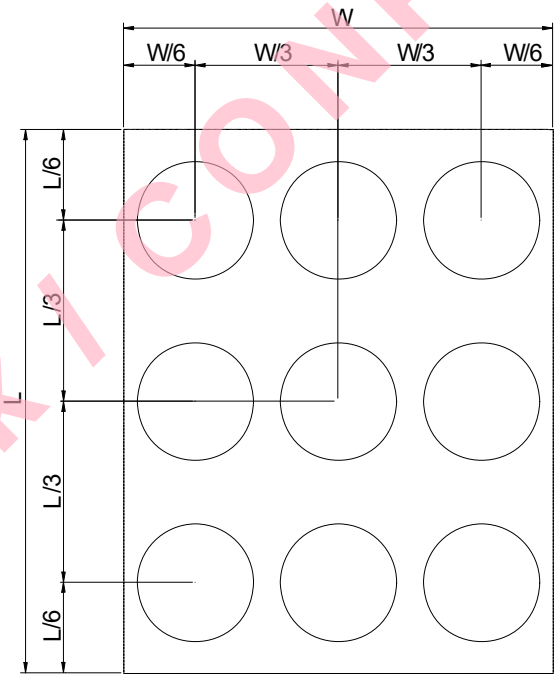


Fig. 5 Definition of luminance uniformity

L_{min} : The measured minimum luminance of all measurement position.

L_{max} : The measured maximum luminance of all measurement position.

8. Reliability Tests

No.	Item	Condition	Criterion
1	High Temperature Storage	80±3℃,120 Hours	No defects in display and operational functions
2	Low Temperature Storage	-30±3℃,120 Hours	
3	High Temperature Operating	70±3℃,120 Hours	
4	Low Temperature Operating	-20±3℃,120 Hours	
5	High Temperature and Humidity Test(Storage)	60±3℃,90±3%RH,120 Hours	
6	Thermal Shock	-30℃(30mins)→80℃(30mins),10Cycle	
7	Electro Static Discharge (Operation)	150pF,330Ω±10KV Contact 150pF,330Ω±15KV Air 5 point/LCM,1time	

Remark:

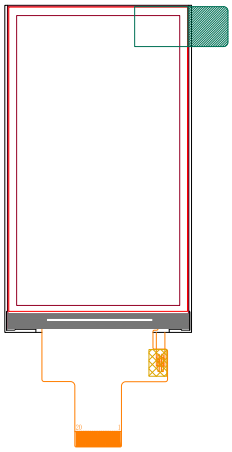
1. The Test samples should be applied to only one test item.
2. Sample for each test item is 2 pcs.
3. The samples must be free from defect before test, must be restored at room condition at least for 2 hours storage at room temperature after reliability test before any inspection.
4. Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
5. After a long period of high temperature, the surrounding edge of the LCM all-black image will appear MURA phenomenon, which is a normal phenomenon.
6. If the product has a temporary performance decline or loss of function during ESD test, and the system returns to normal display after reset, it is judged to be OK.

9. Package Drawing

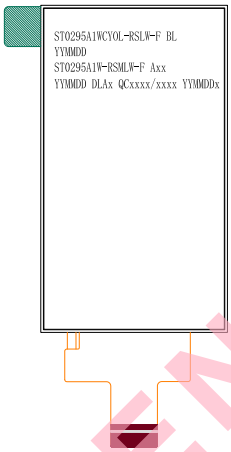
TBD

10. Incoming Inspection Specification

10.1 Product Configuration



Front view



Rear view

10.2 Acceptable Criteria

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD=105.

a. Lot size: Quantity per shipment as one lot (Different model as different lot).
b. Sampling type: Normal inspection, single sampling.
c. Sampling level: II
d. AQL: Acceptable quality level
   - Major defect: 0.65
   - Minor defect: 1.0

10.3 Classification of defects

Defects are classified 2 types, major defect and minor defect according to the defects. The definition of defects is classified as below:

a. Major defect
   Any defect may result in functional failure, or reduce the usability of product for its purpose. For example, electrical failure, deformation and etc..
b. Minor defect
   A defect that is not to reduce the usability of product for its intended purpose and inconsistency, dot defect and etc..
   The criteria on major or minor judgment will be according with the classification of defects.

10.4 The environment condition of inspection

The environmental condition and visual inspection shall be conducted as below:

a. Ambient temperature: 25+/-5℃
b. Humidity: 25%~75%RH
c. Panel visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm~40cm or more between the LCD module and eyes of inspector.
   Ambient illumination: 700Lux~1000Lux for external appearance inspection
   Ambient illumination: 300+/-50Lux for light on inspection

d. The viewing angle when inspection:
- +/-30 degrees to the surface of display panel in vertical direction. (See Figure 1)

e. Display panel shall be conducted at the distance 30cm~40cm between the LCD module and eyes of inspector (See Figure 2)

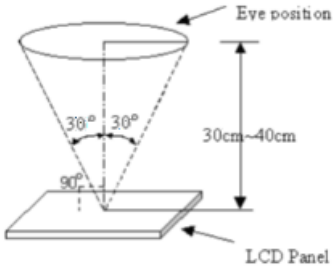


Figure 1

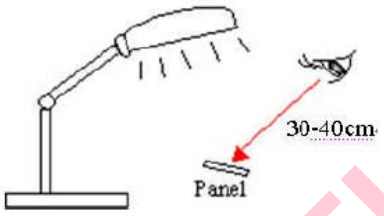


Figure 2

f. Application of ND filter
Put ND filter in front of the defects with height 2.5 cm ~3cm, and view the defect through ND filter in vertical direction with viewing distance 30cm~40cm. (See Figure 3)

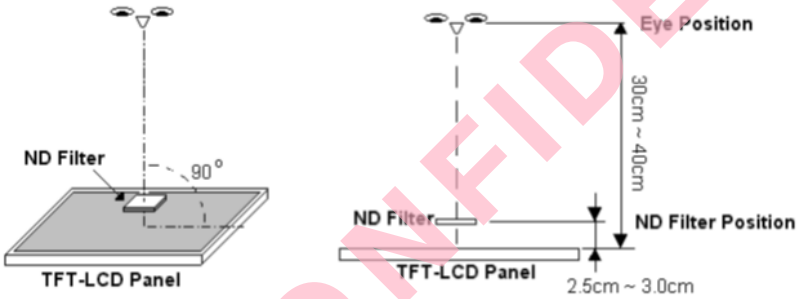
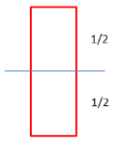
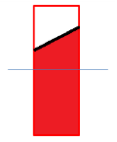
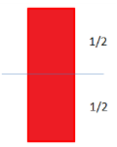


Figure 3

10.5 Inspection Criteria

a. Definition of dot defect induced from the panel inside
- The Bright or dark dot that comply with both following conditions is considered as bright dot or dark dot:
i. Bright or dark dot size is more than 50% of 1 dot;

Explanation	Example	Judge
Neither bright dot nor dark dot		OK
Effected area of Sub-pixel is less than ½ total area.		Ignored and the size if less than 50% of 1 dot size.
Effected area of Sub-pixel is more than ½ total area.		Judge as dots, and judge it according to specification
Effected area of Sub-pixel is more than ½ total area.		Judge as dots, and judge it according to specification

ii. Visible under 5% ND filter;

- Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
- Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green blue picture.
- 2 dot adjacent=1 pair =2 dots (See figure 4)

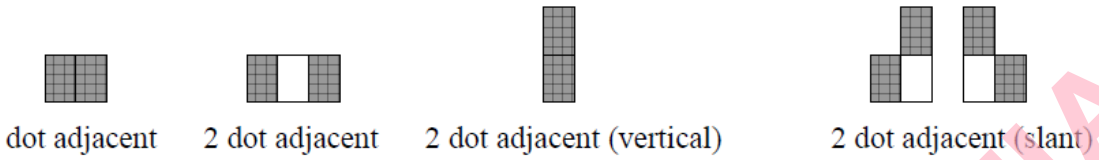


Figure 4

b. Bright and dark dots when display inspection (If visible under 5%ND filter, judge follows following specification)

Items		Acceptable count
Bright dot	Random	N≤1
Dark dot	Random	N≤2
	2 dots adjacent	N≤1
	3 dots adjacent	N≤0
Total dots(Including bright and dark dots)		N≤3
Tiny bright dot		Ignored if invisible through 5%ND filter, If visible through 5% ND filter, D≤0.15MM, Ignored 0.15mm<D≤0.2mm, N≤3

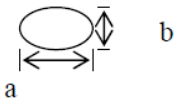
c. Appearance & display inspection

Condition	Item	Standards
Display on	Foreign black/White/Bright spot (Display & appearance)	D≤0.2mm, Ignored 0.2mm<D≤0.3mm, N≤2 It is shown in figure 5.
	Foreign black/White/Bright line (Display & appearance)	W≤0.07mm, ignored 0.07<W≤0.1mm, L≤3.0mm, N≤4 It is shown in figure 6.
	Mura/Waving/white spot and etc…	Ignored if invisible through 5%ND filter in black or white picture. If visible, judged according to circular defects. Or judge by limited sample if necessary.
Display off	Surface dent/Air Bubble/Fish eyes	D≤0.2mm, Ignored 0.2mm<D≤0.3mm, N≤2 It is shown in figure 5.
	Surface scratches	W≤0.07mm, ignored 0.07<W≤0.1mm, L≤3.0mm, N≤4.

Remark:

Defects which are outside of Active area are not considered as a defect.

1. W：Width
2. L：Length
3. D：Average Diameter
4. N：Count



D=(a+b)/2

Figure 5

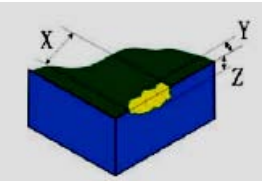
W: width, L：length

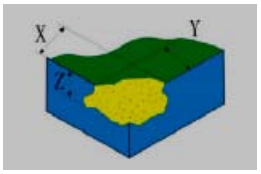
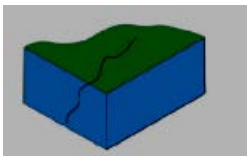
Figure 6

d. Function inspection

Item	Standards
Display failure (V-line/H-Line/Cross line, etc..)	Not allowed.
Touching function failed	Not allowed.
No display	Not allowed.
Abnormal display (Flickering, discolor, etc..)	Not allowed.

10.6 External Appearance Inspection Criteria

Item	Contents	
TP and logo color	Spec follows the pantone code which defined in drawing. Judge according to limit samples.	
FPC Cable	Cable not continuous, break-off, connector burn-off/Damaged are not acceptable. Visual problems, crease, folding trace, surface dirt, scratches and other minor visual problems, if they don't affect the function, acceptable.	
Backlight	Scratch	The scratch which may causes a problem in practical use is not allowed.
	Break off	Breaking off is not allowed.
	Crack	Any crack is not allowed.
Stain on surface	The stain which can't be clean is not allowed, otherwise, it is acceptable.	
Tape/label	Incorrect position or missing label is not allowed.	
Connector	Assembly NG or function failure caused by deformation is not allowed. Oxidation or discolor at the gold fingers area by eyes are not allowed.	
Dimensions	In specification according to drawing.	
Soldering	Follow IPC-A-610, Level 2.	
Marking	Visible and legible are acceptable, illegible or unclear is not allowed.	
Logo/printing/ink	Clear and legible, discolor, illegible, pinholes are not allowed by eyes.	
Chipping at TP edge	- Chipping is visible from viewing side (From front side) by eyes, not allowed. - Chipping at back side, judge refers to following: A. Chipping at the edge: 	

	X ≤0.5mm ,Y ≤ 0.5mm, Z ≤1/2t, acceptable. X>0.5mm, Y>0.5mm, not allowed. B. Chipping at the corner  X ≤0.5mm ,Y ≤ 0.5mm, Z ≤1/2t, acceptable. X>0.5mm, Y>0.5mm, not allowed.
Extended Cracking	Not allowed 

Remark:

If any defect is not defined in the above standard, it should be judged after discussion.

11. Cautions

a. Recommended Storage condition: Temperature: 25ºC+/-5ºC, Humidity: ≤75%RH. Clear and free with dust and flowing particles space.

b. Don't disassemble and reassemble the module by yourself.

c. Acid, alkali, alcohol or touched directly by hand will damage the display.

d. Static electricity will damage the module. Please configure grounding device. And enough anti-statics protection when touching products.

e. The strong vibration, shock, twist or bend will cause material damage, even module broken.

f. It is easy to cause image sticking while displaying the same pattern for very long time.

g. The response time, brightness and performance will vary from different temperature.

h. LCD Devices are made of fragile material such as Glass and may be broken or cracked if dropped it, so please handle them with care. Please be careful not to cut your hand if you break the glass.

i. Do not stack the LCDs to avoid the LCDs damage and contamination.

j. Before using the LCDs, please check the specification.

k. LCDs contain a small amount of Liquid Crystal. Please follow local ordinances or regulations for disposal.

l. LCD shall be stored in same packing material during import, and under the condition of room temperature (20-30 degree C).

m. Please do not leave LCD modules under the direct sunlight or strong infra-red radiation for a long period time to prevent liquid crystal deteriorating.

n. Please turn off the power supply before plugging or unplugging LCD module.

o. Please do not rub, push, or hit LCD surface with hard tool etc. Film on surface is easily scratched, when droplets of water or dirt are on the surface, please gently remove them with soft fabric.

p. Handling of main and LED FPC (Flexible Printed Circuit), please be careful, do not strongly pull or scratch FPC, to avoid failure of the components and bonding part.

12. Limited Warranty

Unless otherwise agreed between Santek and customer, Santek will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with Santek LCD acceptance standards(copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to Santek within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Santek limited to repair and/or replacement on the terms set forth replacement on the terms setforth above. Santek shall not be responsible for any subsequent or consequential events.

12.1 Returning LCM Under Warranty –Terms and Conditions

a. No warranty can be granted if the precautions stated above have been disregarded.
The typical examples of violations are:
- Broken LCD glass.
- Circuit modified in any way, including addition of components.

b. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB's eyelet, conductors and terminals.