珠海三泰克科技有限公司

San Technology (Zhuhai) Co., Ltd.

# SPECIFICATION
# FOR
# LCD Module

**Customer P/N:**

**Santek P/N: ST0256A2W-RSMLW-C**

**DOC. Revision: RS01**

**Customer Approval:**

| | |
|---|---|
| | |

| | SIGNATURE | DATE |
|---|---|---|
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| CHECKED BY | Aaron Lu Andy Song | 2022-09-13 |
| APPROVED BY | Natty Lee | 2022-09-13 |

Document Revision History

| Version | Revise Date | Description | Changed by |
|---|---|---|---|
| RS01 | 2022-09-13 | First issue | Jerry Yang |

# Table of Contents

# 1. GENERAL DESCRIPTION

1.1 Application

This data sheet is to introduce the specification of active matrix 16,777,216 color LCD module.
Main color LCD module is controlled by Driver IC (Synaptics VHIR63455++-WS).
If any problem occur s concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

1.2 Construction and Outline

This module is a color transmissive, high contrast, wide viewing angle and active matrix LCD module.
Construction: LCD panel, Driver (COG), FPC with electric components, LEDs, prism sheet, diffuser, light guide, reflector and plastic frame to fix them mechanically.

1.3 Mechanical Specification

Table 1

| Item | Specifications | Unit | Remarks |
|---|---|---|---|
| Screen size (Diagonal) | 2.56inch | mm | |
| Active area | 46.008(H) x 46.008(V) | mm | |
| Pixel format | 2160(H) x 2160 (V) | Pixel | |
| | 1 Pixel =R+G+B dots | - | |
| Pixel pitch | 21.3 (H) x 21.3(V) | μm | |
| Pixel configuration | R,G,B Vertical Stripes | - | |
| Display mode | Normally Black | - | |
| Number of colors | 16,777,216 | Colors | 24 bits |
| Outline dimensions | 50.51 (W) x 57.49 (H) x 1.92 (D) | mm | Note 3-1 |
| Mass | About 10 | g | |

Note 3-1) The above-mentioned table indicates module sizes without some projections and FPC

1.4 Pixel Configuration

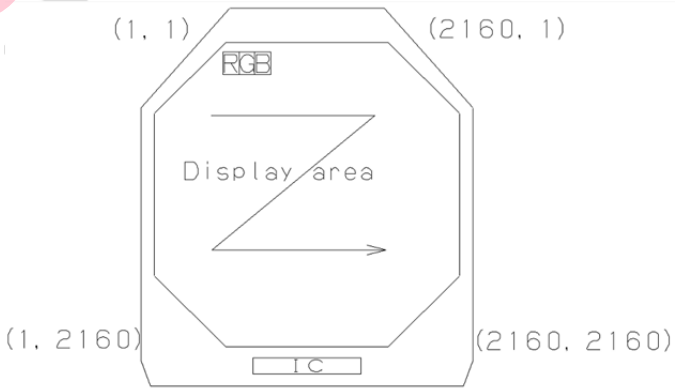
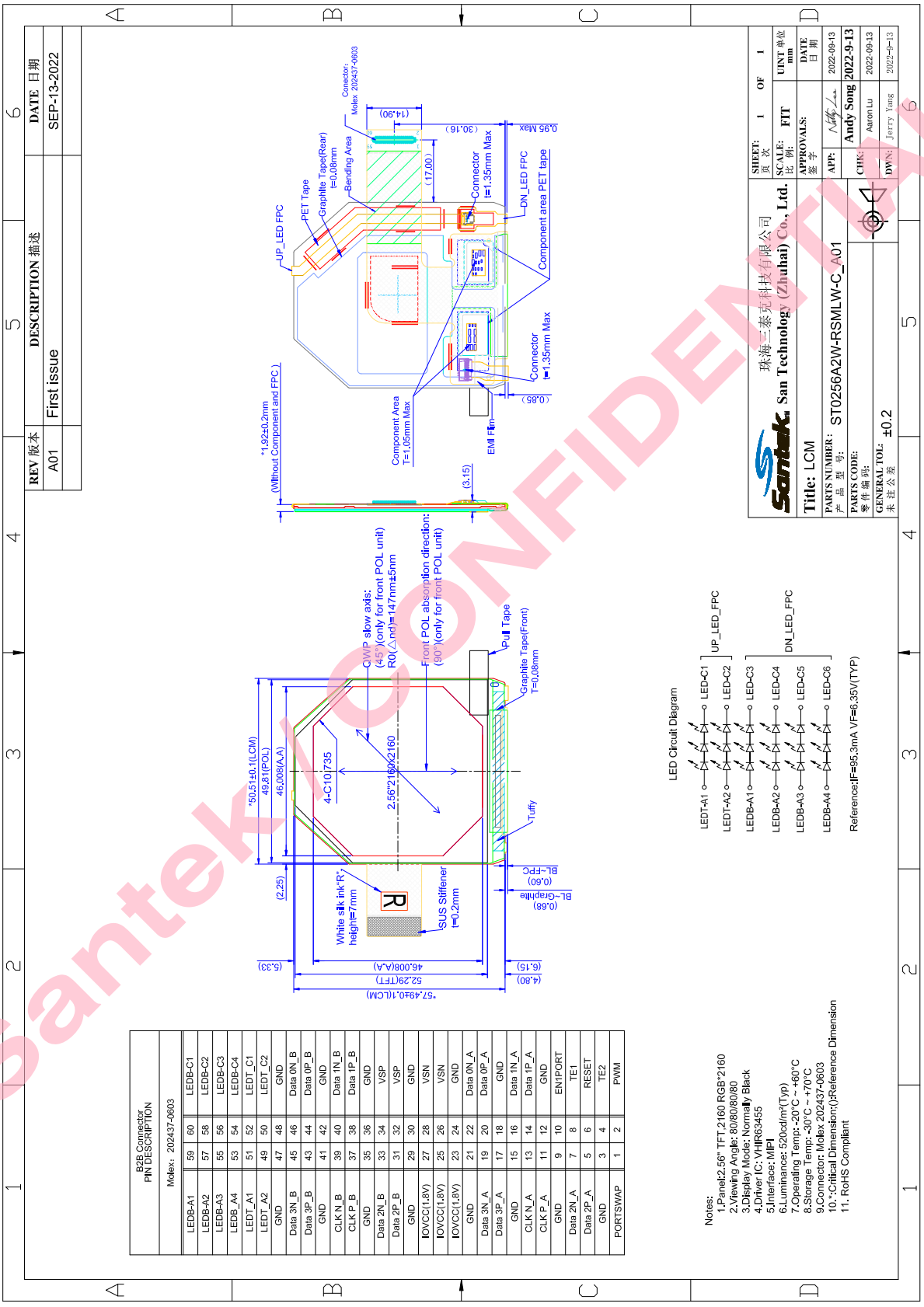



Fig.1

## 2. MECHANICAL DRAWING



# 3. INTERFACE CONNECTION

3.1 Input Terminal Names and Functions

Table2

| Pin No | Signal | Function | I / O |
|---|---|---|---|
| 1 | PORTSWAP | Selects the master port ("H"=port B, "L"=port A) | I |
| 2 | PWM | Control signal for LED backlight (refer to next page) | O |
| 3 | GND | GND=0V | - |
| 4 | TE2 | Tearing effect output | O |
| 5 | Data 2P_A | Mipi data2 positive signal of MIPI Port A | I |
| 6 | RESET | Reset pin (Low active) | I |
| 7 | Data 2N_A | Mipi data2 negative signal of MIPI Port A | I |
| 8 | TE1 | Tearing effect output | O |
| 9 | GND | GND=0V | - |
| 10 | EN1PORT | selects the number of DSI-2 ports("H"=1 port "L"= 2 port) | I |
| 11 | CLK P_A | Mipi clock positive signal of MIPI Port A | I |
| 12 | GND | GND=0V | - |
| 13 | CLK N_A | Mipi clock negative signal of MIPI Port A | I |
| 14 | Data 1P_A | Mipi data1 positive signal of MIPI Port A | I |
| 15 | GND | GND=0V | - |
| 16 | Data 1N_A | Mipi data1 negative signal of MIPI Port A | I |
| 17 | Data 3P_A | Mipi data3 positive signal of MIPI Port A | I |
| 18 | GND | GND=0V | - |
| 19 | Data 3N_A | Mipi data3 negative signal of MIPI Port A | I |
| 20 | Data 0P_A | Mipi data0 positive signal of MIPI Port A | I / O |
| 21 | GND | GND=0V | - |
| 22 | Data 0N_A | Mipi data0 negative signal of MIPI Port A | I / O |
| 23 | IOVCC(1.8V) | Power supply to the logic circuit (1.8V) | I |
| 24 | GND | GND=0V | - |
| 25 | IOVCC(1.8V) | Power supply to the logic circuit (1.8V) | I |
| 26 | VSN | Power supply to the analog circuit (-5.8V) | I |
| 27 | IOVCC(1.8V) | Power supply to the logic circuit (1.8V) | I |
| 28 | VSN | Power supply to the analog circuit (-5.8V) | I |
| 29 | GND | GND=0V | - |
| 30 | GND | GND=0V | - |
| 31 | Data 2P_B | Mipi data2 positive signal of MIPI Port B | I |
| 32 | VSP | Power supply to the analog circuit (5.8V) | I |
| 33 | Data 2N_B | Mipi data2 negative signal of MIPI Port B | I |
| 34 | VSP | Power supply to the analog circuit (5.8V) | I |
| 35 | GND | GND=0V | - |
| 36 | GND | GND=0V | - |
| 37 | CLK P_B | Mipi clock positive signal of MIPI Port B | I |
| 38 | Data 1P_B | Mipi data1 positive signal of MIPI Port B | I |
| 39 | CLK N_B | Mipi clock negative signal of MIPI Port B | I |
| 40 | Data 1N_B | Mipi data1 negative signal of MIPI Port B | I |
| 41 | GND | GND=0V | - |

| | | | |
|---|---|---|---|
| **42** | GND | GND=0V | - |
| **43** | Data 3P_B | Mipi data3 positive signal of MIPI Port B | I |
| **44** | Data 0P_B | Mipi data0 positive signal of MIPI Port B | I / O |
| **45** | Data 3N_B | Mipi data3 negative signal of MIPI Port B | I |
| **46** | Data 0N_B | Mipi data0 negative signal of MIPI Port B | I / O |
| **47** | GND | GND=0V | - |
| **48** | GND | GND=0V | - |
| **49** | LEDT_A2 | LEDT anode 2 | I |
| **50** | LEDT_C2 | LEDT cathode 2 | I |
| **51** | LEDT_A1 | LEDT anode 1 | I |
| **52** | LEDT_C1 | LEDT cathode 1 | I |
| **53** | LEDB_A4 | LEDB anode 4 | I |
| **54** | LEDB-C4 | LEDB cathode 4 | I |
| **55** | LEDB-A3 | LEDB anode 3 | I |
| **56** | LEDB-C3 | LEDB cathode 3 | I |
| **57** | LEDB-A2 | LEDB anode 2 | I |
| **58** | LEDB-C2 | LEDB cathode 2 | I |
| **59** | LEDB-A1 | LEDB anode 1 | I |
| **60** | LEDB-C1 | LEDB cathode 1 | I |

Matching Connector : Molex:202437-0603

# 4. ABSOLUTE MAXIMUM RATINGS

Table3 GND=0V

| Parameter | Symbol | Conditions | Rated Value | Unit | Remarks |
|---|---|---|---|---|---|
| Driver IC (Positive Analog) Power Supply Voltage | VSP | Ta=+25°C | -0.3 to +6.5 | V | Note1 |
| Driver IC (Negative Analog) Power Supply Voltage | VSN | Ta=+25°C | +0.3 to -6.5 | V | Note1 |
| Driver IC (Digital) Power Supply Voltage | VDDIO | Ta=+25°C | -0.3 to +2.3 | V | Note1 |
| Temperature for storage | $T_{stg}$ | - | -30 to +70 | °C | Note2 |
| Temperature for operation | $T_{opr}$ | - | −20 to +60 | °C | Note2 |
| LED Input electric current | ILED | Ta=+25°C | 0 to 100 (Duty 10%) | mA | Note3 |

Note1: Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V). Always connect all GND externally and use at the same voltage.

Note2: Humidity: 95%RH Max.(at T*a*≤40°C). Maximum wet-bulb temperature is less than 39°C (at T*a*>40°C). Condensation of dew must be avoided.

Note3: Ambient temperature and the maximum input are fulfilling the following operating conditions.

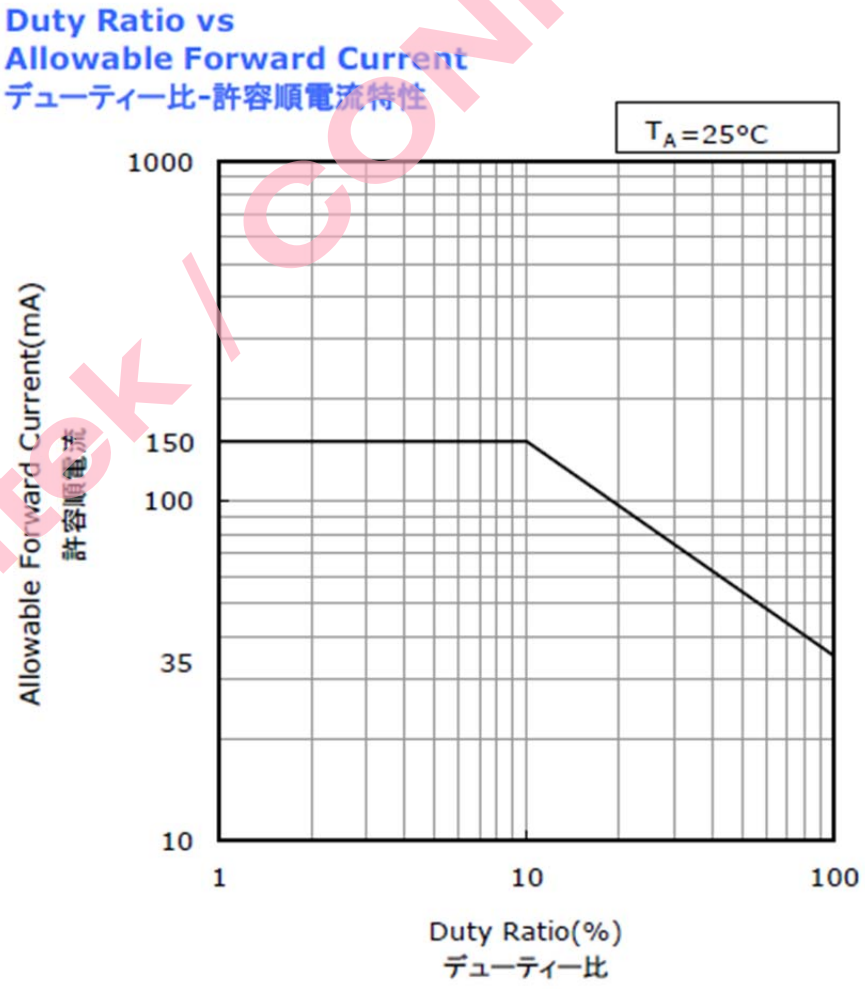



Fig. 2

# 5. ELECTRICAL SPECIFICATIONS

5.1 TFT-LCD Panel Driving Section

Table4

Ta=+25°C, GND=0V

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Driver IC(Digital) Power Supply Voltage | VDDIO | 1.7 | 1.8 | 1.9 | V | Note1 |
| Driver IC(Positive Analog) Power Supply Voltage | VSP | 5.7 | 5.8 | 5.9 | V | Note1 |
| Driver IC(Negative Analog) Power Supply Voltage | VSN | -5.9 | -5.8 | -5.7 | V | Note1 |
| Input voltage (Low) | $V_{IL}$ | 0 | - | 0.3 VDDIO | V | Note2 |
| Input voltage (High) | $V_{IH}$ | 0.7 VDDIO | - | VDDIO | V | Note2 |
| Input current (Low) | $I_{IL}$ | -10 | - | - | μA | |
| Input current (High) | $I_{IH}$ | - | - | 10 | μA | |
| Output voltage (Low) | $V_{OL}$ | 0 | - | 0.2 VDDIO | V | $I_{OL}$=+0.1mA |
| Output voltage (High) | $V_{OH}$ | 0.8 VDDIO | - | VDDIO | V | $I_{OH}$=-0.1mA |
| Current consumption | $I_{VDDIO}$ | - | 100.2 | 129.6 | mA | Note3 |
| | $I_{VSP}$ | - | 16.4 | 23.8 | mA | |
| | $I_{VSN}$ | - | 14.1 | 21.1 | mA | |

Note1: Include Ripple Noise

Note2: Applied overshoot

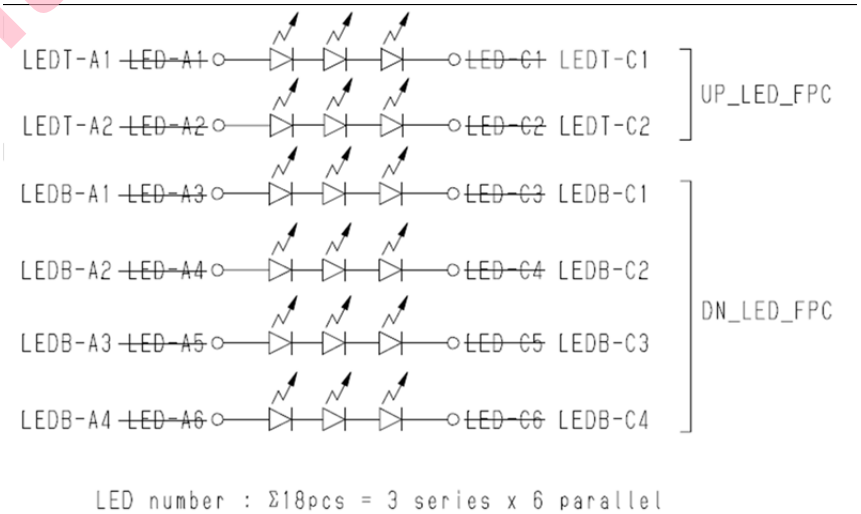
Note3: 120Hz / D-phy 4lane /FIFO mode/ with 1/3DSC / White pattern

5.2 Back Light Driving Section

Table5

Ta=+25°C, GND=0V

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| LED Voltage | $V_{LED}$ | - | 6.35 | - | V | per unit(Duty10%) |
| LED Current | $I_{LED}$ | - | 95.3 | - | mA | Duty 10% |
| Power Consumption | $W_{LED}$ | - | 8.1 | - | | Duty 100% |
| LED Quantity | | 18 | | | pcs | |




LED number : Σ18pcs = 3 series x 6 parallel

# 6. TIMING CHARACTERISTICS OF INPUT SIGNALS

6.1. MIPI DC/AC Characteristics

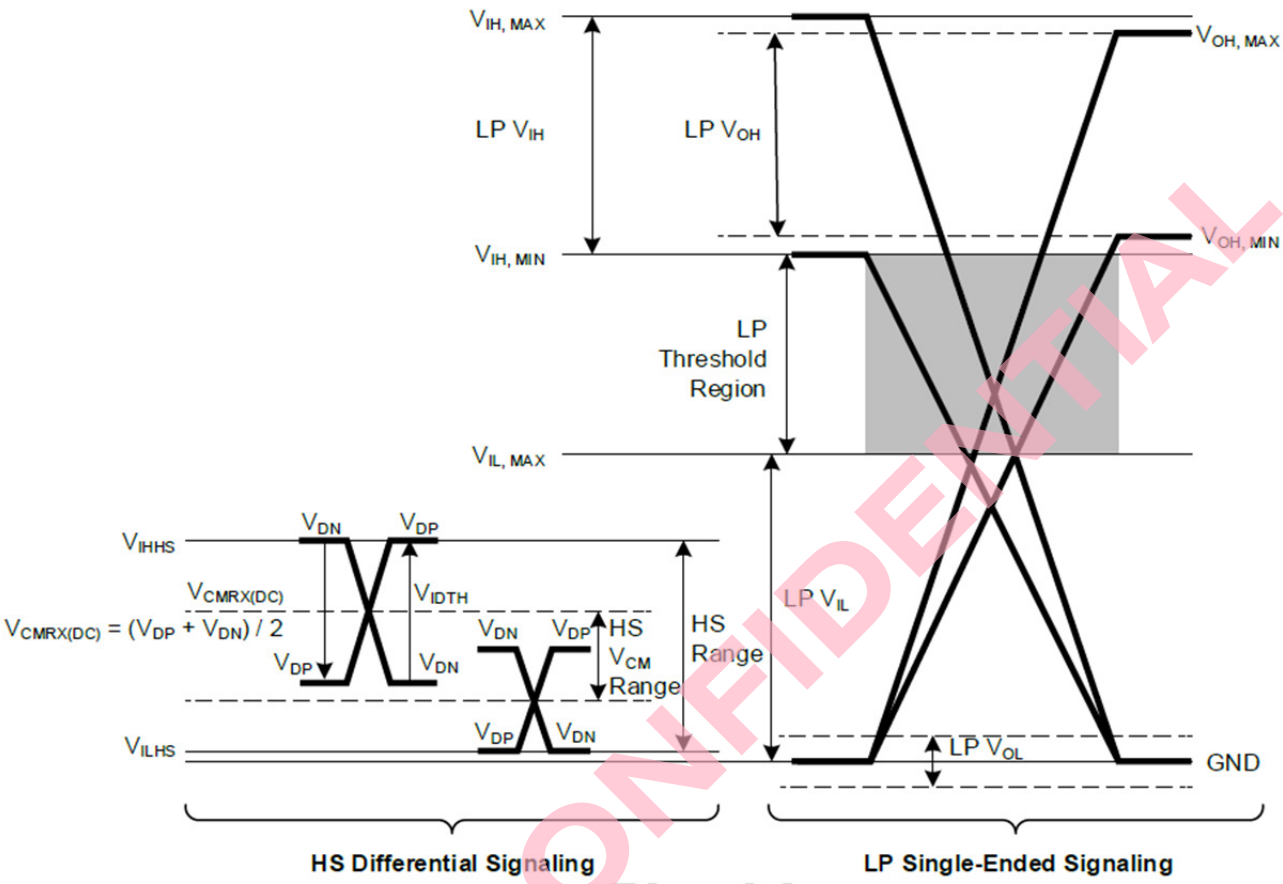
<DC characteristics>

MIPI DSI characteristics

Table6

| Item | | Symbol | Unit | Test Condition | Minimum | Typical | Maximum |
|---|---|---|---|---|---|---|---|
| HS-RX | Differential input high threshold | VIDTH | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | – | – | 70 |
| | Differential input low threshold | VIDTL | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | -70 | – | – |
| | Single-ended input low voltage | VILHS | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | -40 | – | – |
| | Single-ended input high voltage | VIHHS | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | – | – | 460 |
| | Common-mode voltage HS receive mode[1] | VCMRX(DC) | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | 70 | – | 330 |
| | Differential input impedance[2] | ZID | Ω | IOVCC = DPHYVCC = 1.65V ~ 1.95V | – | 100 | – |
| LP-RX | Logic 0 input voltage not in ULP State | VIL | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | -50 | – | 550 |
| | Logic 1 input voltage | VIH | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | 880 | – | 1350 |
| | I/O leakage current | ILEAK | µA | Vin = -50 mV – 1350 mV | -10 | – | 10 |
| LP-TX | Thevenin output low level | VOL | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | -50 | – | 50 |
| | Thevenin output high level | VOH | V | IOVCC = DPHYVCC = 1.65V ~ 1.95V | 1.1 | 1.2 | 1.3 |
| | Output impedance of LP transmitter[2] | ZOLP | Ω | IOVCC = DPHYVCC = 1.65V ~ 1.95V | 110 | – | – |
| CD-RX | Logic 0 contention threshold | VILCD | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | – | – | 200 |
| | Logic 1 contention threshold | VIHCD | mV | IOVCC = DPHYVCC = 1.65V ~ 1.95V | 450 | – | – |

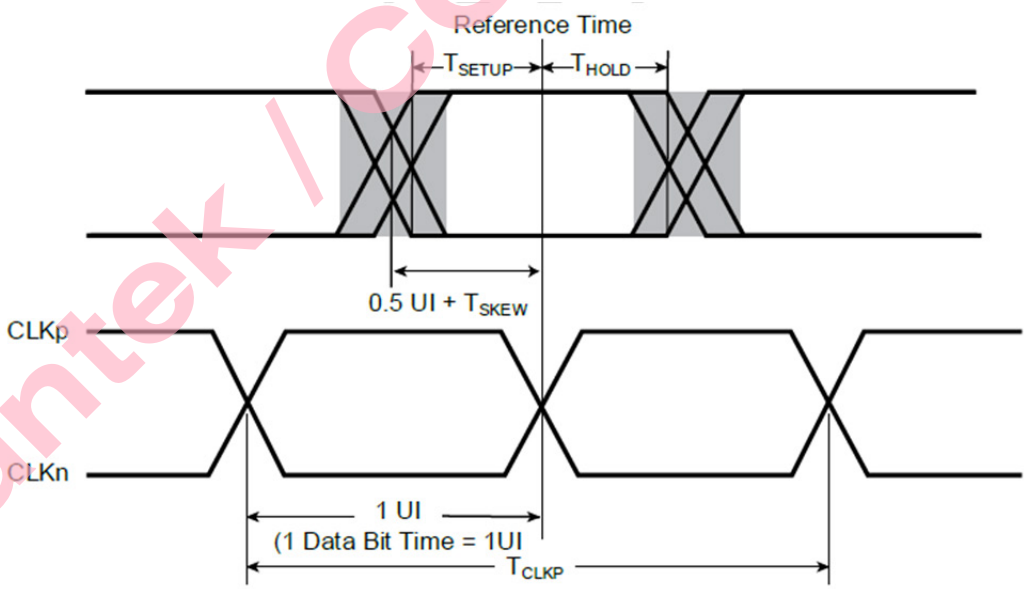
1. VCMRX (DC) = (VDP+VDN)/2
2. Excluding COG resistance (contact resistance and indium tin oxide (ITO) wiring resistance)



<AC Characteristics>
MIPI DSI HS-RX Clock and Data-Clock Specifications
Table7

| Item | Symbol | Unit | Test Condition | Minimum | Typical | Maximum | Footnote |
|---|---|---|---|---|---|---|---|
| DSICLK frequency | fDSICLK | MHz | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 250 | — | 750 | 1 |
| DSICLK cycle time | tCLKP | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 1.33 | — | 4 | 1 |
| DSI data transfer rate | tDSIR | Mbps | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 500 | — | 1500 | 1 |
| Data to clock setup time | tSETUP | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps | 0.15 | — | — | 1, 3 |
| | | ns | | 0.15 | — | — | 1, 2, 3 |
| | | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps | 0.2 | — | — | 1, 3 |
| | | ns | | 0.13 | — | — | 1, 2, 3 |
| Clock to data hold time | tHOLD | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps | 0.15 | — | — | 1, 3 |
| | | ns | | 0.15 | — | — | 1, 2, 3 |
| | | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps | 0.2 | — | — | 1, 3 |
| | | ns | | 0.13 | — | — | 1, 2, 3 |

1. Minimum 110 mV/-110 mV HS differential swing is required for display data transfer.
2. tSETUP/tHOLD times are measured without HS-TX jitter.
3. Minimum tSETUP/tHOLD Time is 0.15 UI or 0.20 UI. This value may change according to the DSI transfer rate.



MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Table8

| Item | Symbol | Unit | Test Condition | Minimum | Typical | Maximum |
|---|---|---|---|---|---|---|
| Time to drive LP-00 to prepare for HS transmission | $T_{HS-PREPARE}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 40 ns + 4 • UI | — | 85 ns + 6 • UI |
| $T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence | $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 145ns + 10 • UI | — | — |
| Time to drive flipped differential state after last payload data bit of a HS transmission burst[1, 2] | $T_{HS-TRAIL}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | max (n • 8 • UI, 60 ns + n • 4 • UI) | — | — |
| Time to drive LP-11 after a HS burst | $T_{HS-EXIT}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 100 | — | — |
| Time to drive LP-00 after a turnaround request | $T_{TA-GO}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 4 • $T_{LPTX}$ | | |
| Time that the new TX waits after the LP-10 state before transmitting the bridge state (LP-00) during a link turnaround | $T_{TA-SURE}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 1 • $T_{LPTX}$ | — | 2 • $T_{LPTX}$ |
| Time that the new TX drives the bridge state (LP-00) after accepting control during a link turnaround | $T_{TA-GET}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 5 • $T_{LPTX}$ | | |
| Length of any low-power state period | $T_{LPX}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 50 | — | — |
| Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between the master and slave sides | Ratio $T_{LPX}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 2/3 | — | 3/2 |
| Time that the transmitter continues sending HS clock after the last associated data lane has transitioned to LP mode[3] | $T_{CLK-POST}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 60 ns + 52 UI | — | — |
| $T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting the clock | $T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 300 | — | — |
| Time that the HS clock is driven prior to any associated data lane beginning the transition from LP to HS mode | $T_{CLK-PRE}$ | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 8 | — | — |
| Time to drive LP-00 to prepare for HS clock transmission | $T_{CLK-PREPARE}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 38 | — | 95 |
| Time to drive HS differential state after last payload clock bit of an HS transmission burst | $T_{CLK-TRAIL}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | 60 | — | — |
| Time from the start of THS-TRAIL period to the start of the LP-11 state[2] | $T_{EOT}$ | — | IOVCC = DPHYVCC = 1.65 ~ 1.95V | — | — | 105 ns + n • 12 • UI |
| Length of the low-power TX period when using the DSI-2 clock[4, 5] | $T_{LPTX1}$ | UI | IOVCC = DPHYVCC = 1.65 ~ 1.95V | — | 1/fTXCLK | — |
| Length of the low-power TX period when using the internal OSC clock[4, 5] | $T_{LPTX2}$ | ns | IOVCC = DPHYVCC = 1.65 ~ 1.95V | — | 8/fosc | — |

1. If a > b then max (a, b) = a, otherwise max (a, b) = b
2. Where n = 1 for forward direction HS mode.
3. R63455 works with this specification, although the last part of the internal process remains when the clock lane enters LP-11 and R63455 works without the remaining process if tCLK-POST is more than 512 UI.
4. R63455 uses the DSI clock from the host processor if the DSI-2 clock lane is active, and uses the internal oscillator clock if the DSI-2 clock lane is stopped.
5. See section "DSI-2 Control Setting (B6h)" (D-PHY) in this document for more information about the DSITXDIV register function.

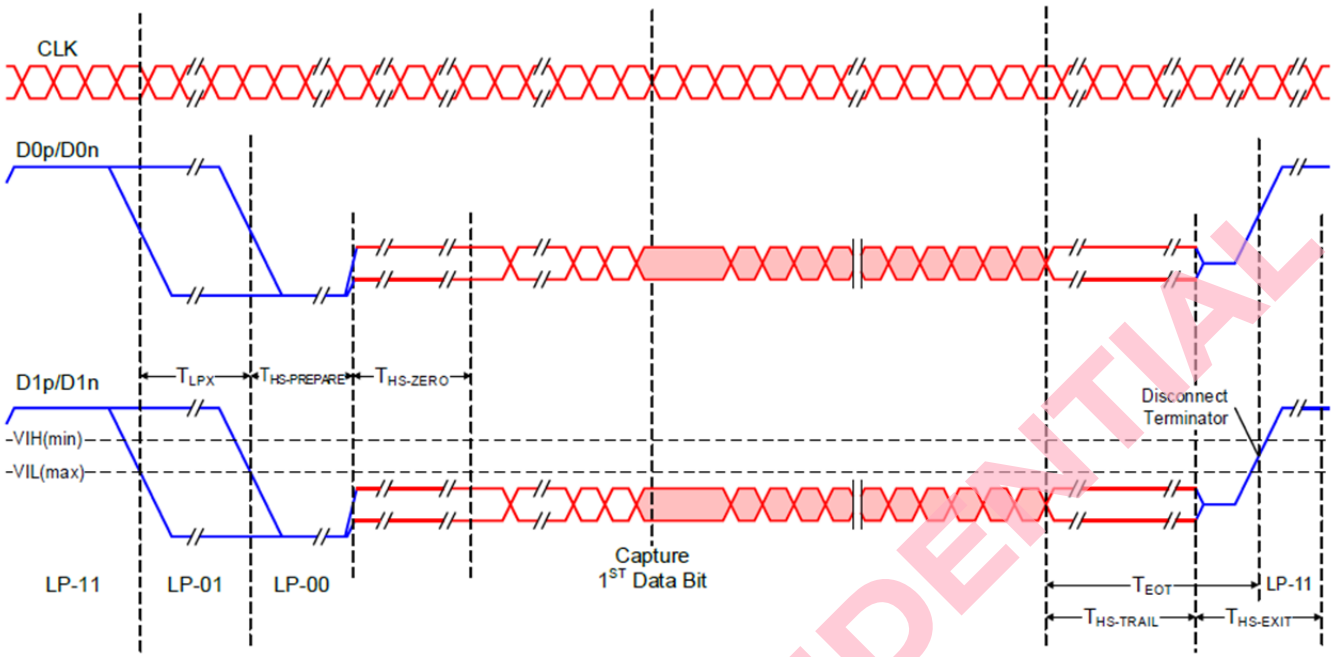



Fig. 5

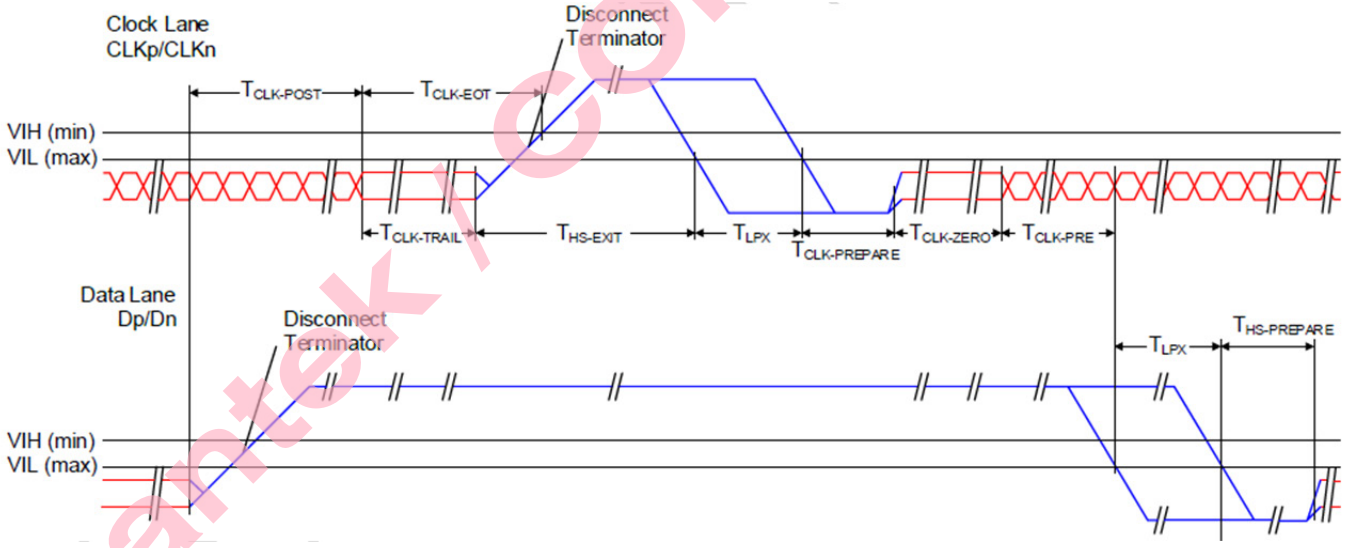



Fig. 6

6.2 Reset Timing Characteristics

Table9

| Item | Symbol | Unit | Test Condition | Minimum | Typical | Maximum |
|---|---|---|---|---|---|---|
| Reset low-level width1 | tRW1 | μs | Power supply on | 3000 | – | – |
| Reset low-level width2 | tRW2 | μs | Operation | 1000 | – | – |
| Reset low-level width3 | tRW5 | ms | Power supply off | 25 | – | |
| Reset to MIPI command | tRT1 | ms | Sleep in | 20 | – | – |
| Noise reject width | tRESNR | μs | – | – | – | 1 |

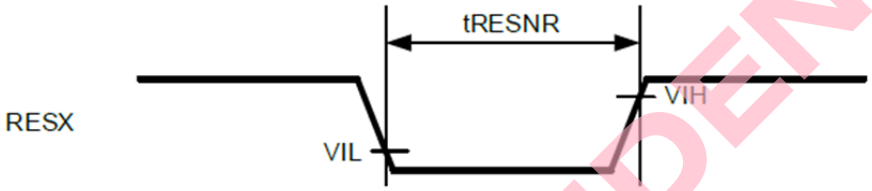



Fig. 7 Reset reject pulse width

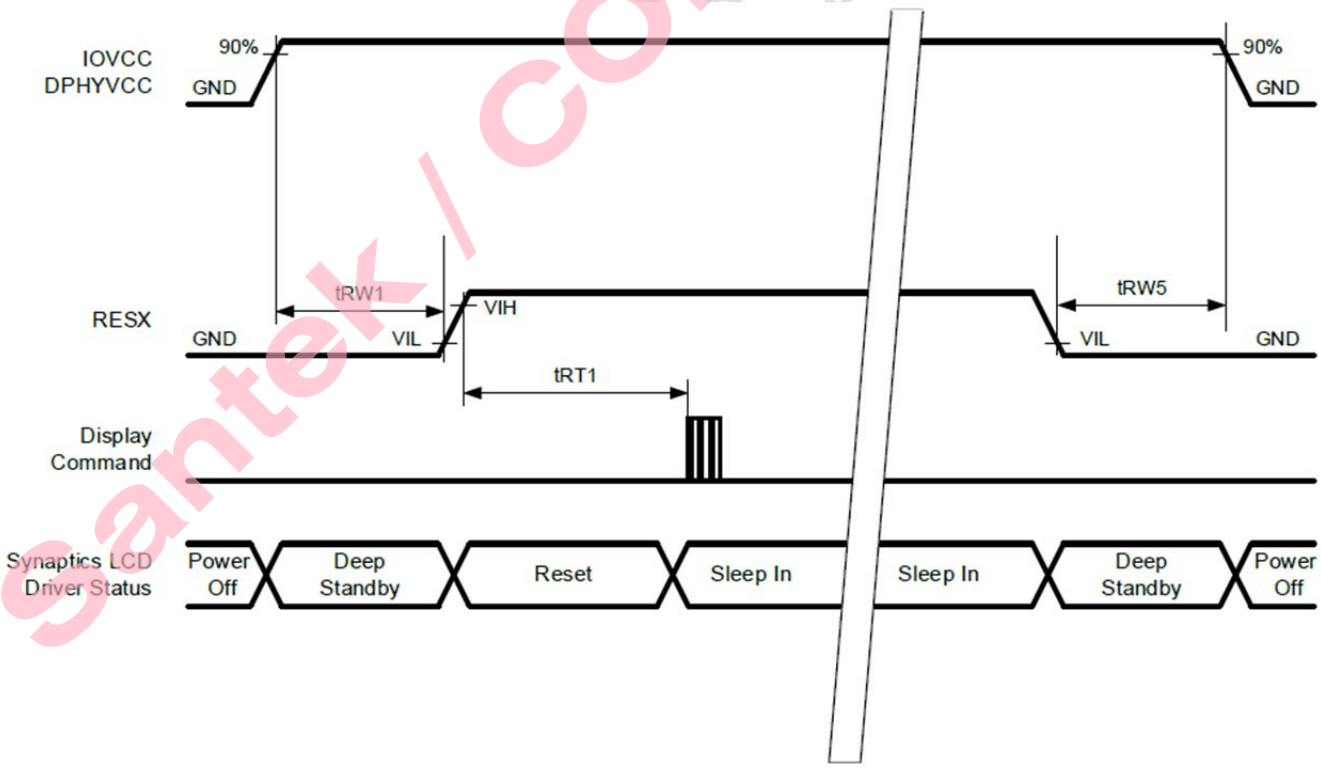



Fig. 8 Reset timing characteristics at power supply on

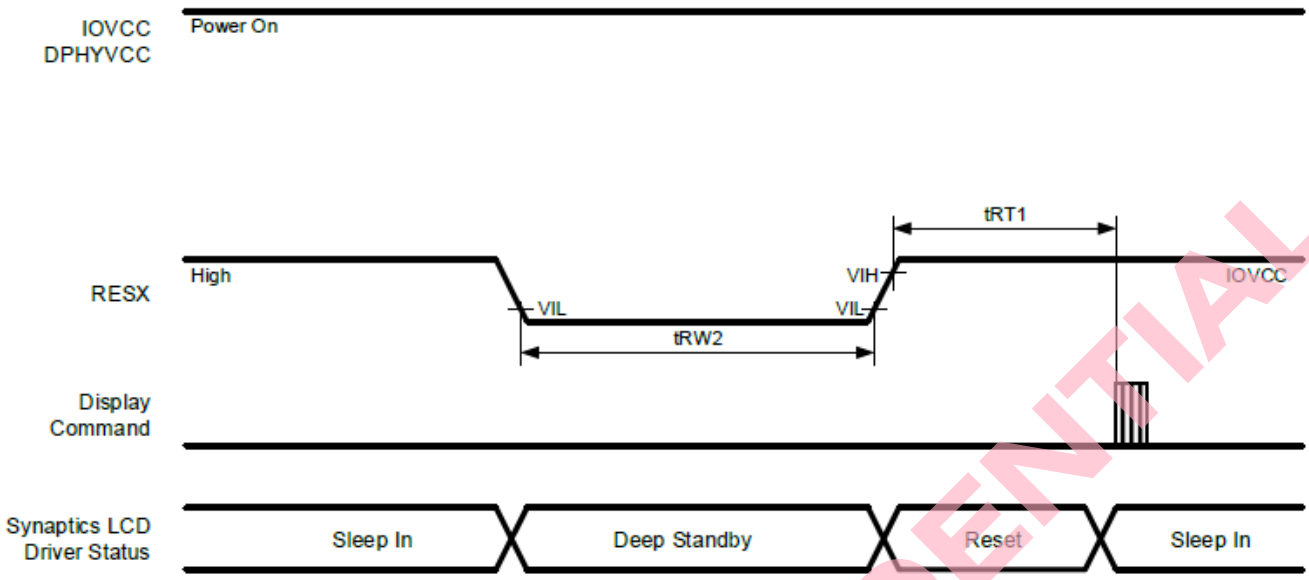



Fig. 9 Reset timing in Sleep in

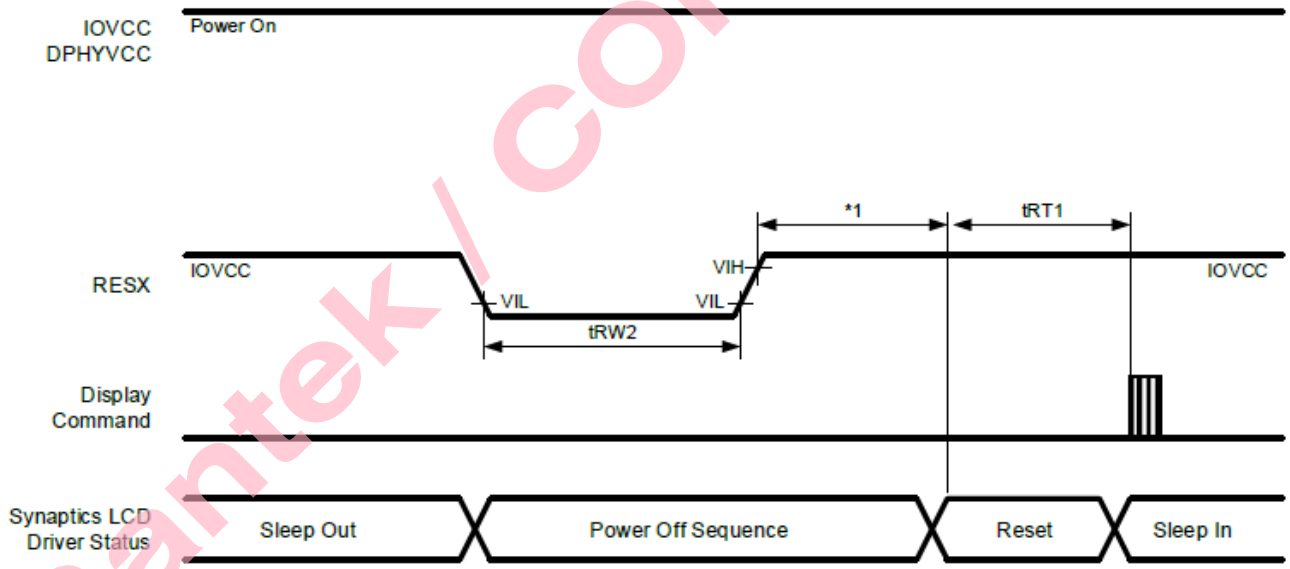



Fig. 10 Reset timing in Sleep out

6.3 Display Timing

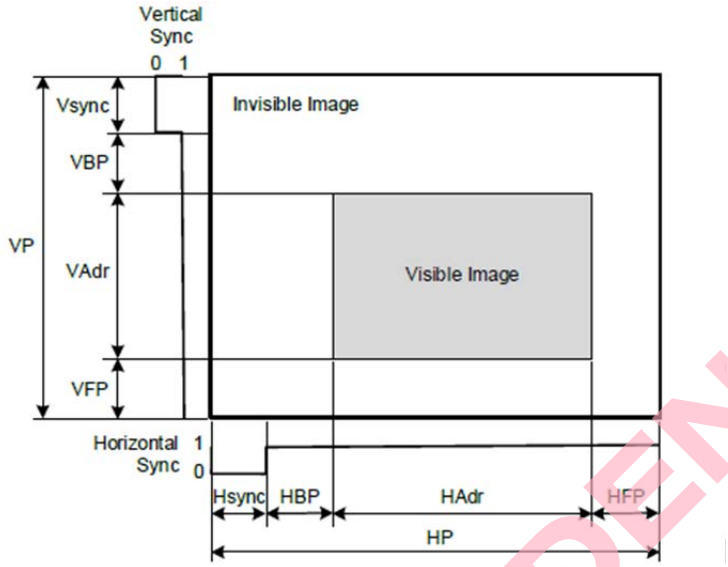



Fig. 11

< Interface Display timing >

Table10 I/F: Mipi 1port 4lane DSC Mode (1/3 Compression), FIFO, Dots Size: 2160xRGBx2160

| Item | | unit | 72Hz | 90Hz | 120Hz |
|---|---|---|---|---|---|
| | Phy | | D-PHY | D-PHY | D-PHY |
| | Port | port | 1 | 1 | 1 |
| | Lane | lane | 4 | 4 | 4 |
| | Transfer Rate (/lane)# | Mbps | 1100 | 1100 | 1270 |
| | PCLK | MHz | 453.97 | 453.97 | 585.66 |
| | input data stream line time | us | 4.994 | 4.994 | 3.837 |
| | Compression Interface | - | DSC 1/3 | DSC 1/3 | DSC 1/3 |
| | | Ver | 1.1 | 1.1 | 1.1 |
| | | Slice_height | 16 | 16 | 16 |
| | Scaling | - | x1.0 | x1.0 | x1.0 |
| | Interface Type | - | FIFO | FIFO | FIFO |
| | VS | line | 4 | 4 | 4 |
| | VFP | line | 613 | 57 | 4 |
| | VBP | line | 4 | 4 | 4 |
| | Vadr | line | 2160 | 2160 | 2160 |
| | HS | pixel | 20 | 20 | 10 |
| | HFP | pixel | 54 | 54 | 54 |
| | HBP | pixel | 33 | 33 | 23 |
| | Hadr | pixel | 2160 | 2160 | 2160 |
| | frame rate | Hz | 72 | 90 | 120 |
| | Burst_mode | - | Non-busrt | Non-busrt | Non-busrt |

#MIPI speed setting is used for Santek JIG, just for reference.

# 7. POWER SEQUENCE

Below shows timing diagram of power on off sequence.

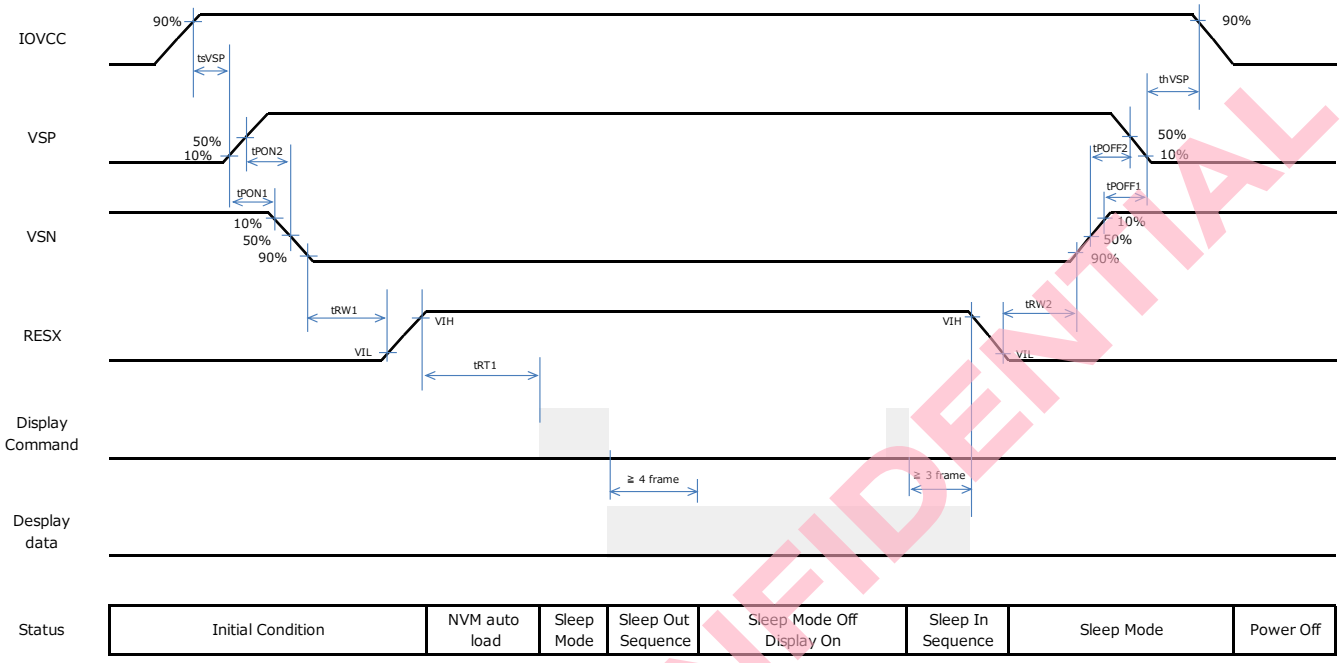



Fig. 12

<Power supply timing characteristics>

Table11

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| VSP-VSN delay time (10% to 10%) | tPON1 | 0 | - | µs |
| VSP-VSN delay time (50% to 50%) | tPON2 | 0 | - | µs |
| System power on to VSP ON time | tsVSP | 1 | - | ms |
| VSN-VSP delay time (10% to 10%) | tPOFF1 | 0 | - | µs |
| VSN-VSP delay time (50% to 50%) | tPOFF2 | 0 | - | µs |
| VSP OFF to system power OFF time | thVSP | 0 | - | µs |

<Reset timing characteristics>

Table12

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Reset low-level width1 | tRW1 | 2 | - | ms |
| Reset low-level width2 | tRW2 | 25 | - | ms |
| Reset to MIPI command | tRT1 | 20 | - | ms |

7.1 Power ON Sequence

Table 13: Recommended Power On Sequence

(1) Power on sequence

| Step | State | Action/Command | I/F (Data Type) | | | Command | Date | |
|---|---|---|---|---|---|---|---|---|
| 1 | Initial Condition | RESX = L | | | | | | |
| 2 | | Power Supply ON : IOVCC,DPHYVCC | | | | | | |
| 3 | | - Wait 10ms | | | | | | |
| 4 | | Power Supply ON : VSP, VSN | | | | | | |
| 5 | | - Wait 10ms | | | | | | |
| 6 | | RESX = H | | | | | | |
| 7 | NVM Auto Load | - Wait 10ms | | | | | | |
| 8 | Sleep Mode On | Manufacture Command Access Protect | DSI | Generic | 6'h29 | **CMD** | 8'hB0 | |
| 9 | | | | | | P1 | 8'h00 | |
| | | | | | | | | |
| 16 | | Generic pin output setting 1 | DSI | Generic | 6'h29 | **CMD** | 8'hB9 | |
| 17 | | (BBL_PWM_1) | | | | P1 | | |
| 18 | | | | | | P2 | | |
| 19 | | | | | | P3 | | |
| 20 | | | | | | P4 | | |
| 21 | | FIFO setting | DSI | Generic | 6'h29 | **CMD** | | |
| 22 | | | | | | P1 | | |
| 23 | | | | | | P2 | | |
| 99 | | NVM Load setting | DSI | Generic | 6'h29 | **CMD** | 8'hD6 | |
| 100 | | | | | | P1 | 8'h00 | |
| 101 | | Manufacture Command Access Protect | DSI | Generic | 6'h29 | **CMD** | 8'hB0 | |
| 102 | | | | | | P1 | 8'h03 | |
| | | set_TE_ON | DSI | DCS | 6'h39 | **CMD** | 8'h35 | |
| | | | | | | P1 | 8'h00 | |
| | | Inversion setting | DSI | DCS | 6'h39 | **CMD** | 8'h36 | |
| | | | | | | P1 | 8'h40 | |
| 103 | | set_gamma_curve | DSI | DCS | 6'h39 | **CMD** | 8'h26 | |
| 104 | | | | | | P1 | 8'h01 | |
| 105 | | get_compression_mode | DSI | DCS | 6'h39 | **CMD** | 8'h03 | |
| 106 | | | | | | P1 | 8'h01 | |
| 107 | | set_display_on | DSI | DCS | 6'h05 | **CMD** | 8'h29 | |
| 108 | | exit_sleep_mode | DSI | DCS | 6'h05 | **CMD** | 8'h11 | |
| 109 | Sleep Out Sequence | - Wait 120ms | | | | | | |
| 110 | | | | | | | | |
| 111 | Sleep Mode Off Display On | | | | | | | |

| | | 72Hz | 90Hz | 120Hz |
|---|---|---|---|---|
| | | Left&Right | Left&Right | Left&Right |
| Different L/R FIFOsetting | BBL CMD | 8'hB9 | | |
| | BBL P1 | 8'h1A | 8'h15 | 8'H0f |
| | BBL P2 | 8'hEF | 8'h8E | 8'h89 |
| | BBL P3 | 8'h02 | 8'h02 | 8'h01 |
| | BBL P4 | 8'hFD | 8'h64 | 8'Hcb |
| | FIFO CMD | 8'hEC | | |
| | FIFO P1 | 8'h05 8'h06 | 8'h05 8'h06 | 8'h04 8'h05 |
| | FIFO P2 | 8'hD8 8'h48 | 8'hD8 8'h48 | 8'hE6 8'h46 |

7.2 Power OFF Sequence

Table 14: Recommended Power Off Sequence

| Step | State | Action/Command | I/F (Data Type) | | | Command | Data |
|---|---|---|---|---|---|---|---|
| 1 | Sleep Mode Off Display On | set_display_off | DSI | DCS | 6'h05 | CMD | 8'h28 |
| 2 | | enter_sleep_mode | DSI | DCS | 6'h05 | CMD | 8'h10 |
| 3 | Sleep In Sequence | - Wait 120ms | | | | | |
| 4 | Sleep Mode On | RESX = L | | | | | |
| 5 | | - Wait 10ms | | | | | |
| | | Power Supply OFF : VSP, VSN | | | | | |
| | | - Wait 10ms | | | | | |
| 6 | | Power Supply OFF : IOVCC,DPHYVCC | | | | | |
| 7 | Power Off | | | | | | |
| | | | | | | | |

# 8. INPUT SIGNALS

Basic Display Colors and Gray Scale of Each Color

Table15 0: Low level voltage, 1: High level voltage

| | Colors & Gray Scale | Gray Scale | Data signals Signal | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | G0 | G1 | G2 | G3 | G4 | G5 | G6 | G7 | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 |
| | | | LSB | | | | | | | MSB | LSB | | | | | | | MSB | LSB | | | | | | | MSB |
| Basic Color | Black | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Green | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Cyan | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Red | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Magenta | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | – | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale of Red | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | GS1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | GS2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | ⇩ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | Brighter | GS253 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇩ | GS254 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | GS255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale of Green | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | GS1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | GS2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | ⇩ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | Brighter | GS253 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇩ | GS254 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | GS255 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale of Blue | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | GS1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | GS2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ⇧ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | ⇩ | ↓ | | | | | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | |
| | Brighter | GS253 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | ⇩ | GS254 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Blue | GS255 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,777,216-color display can be achieved on the screen. screen.

# 9. OPTICAL CHARACTERISTIC

Table16 VDDI=1.8V, AVDD=5.8V, AVEE=-5.8V, Frame Frequency = 72fps, ILED=95.3mA@10%Duty, Ta = 22°C(±3°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Contrast Ratio | CR1 | θ=0° | 500 | 650 | - | - | Note11-1，2 |
| Response Time | τ | θ=0° | - | – | 4 | Ms “0-255" or "255-0” | Ta=+25°C Note11-3 |
| | | | - | - | 5 | Ms GTG（0~127） | Ta=+25°C Note11-3 |
| White Chromaticity | x | θ=0° | 0.272 | 0.297 | 0.322 | - | - |
| | y | | 0.288 | 0.313 | 0.338 | - | |
| Red Chromaticity | x | | 0.633 | 0.658 | 0.683 | - | |
| | y | | 0.309 | 0.334 | 0.359 | - | |
| Green Chromaticity | x | | 0.274 | 0.299 | 0.324 | - | |
| | y | | 0.632 | 0.657 | 0.682 | - | |
| Blue Chromaticity | x | | 0.126 | 0.151 | 0.176 | - | |
| | y | | 0.029 | 0.054 | 0.079 | - | |
| Chromaticity Uniformity | | - | - | - | ±0.015 | Δu’v’ | 9 point,V255 |
| Brightness | L | θ=0° | - | 520 | - | cd/m² | - |
| Color shift | - | θ=30° | - | - | ±0.02 | Δu’v’ | Note11-1,V255 |
| Uniformity | U | θ=0° | 70 | - | - | % | Note11-4 |
| NTSC Ratio | S | θ=0° | 78.5 | 84 | - | % | Note11-1 |
| Surface Reflectence | SCI | θ=0° | - | 2.0% | 2.5% | - | @550nm |
| Gamma | γ | θ=0° | 2 | 2.2 | 2.4 | - | *1), Note11-1 |
| Flicker | F | θ=0° | - | - | -20 | dB | Note11-5 |
| Crosstalk | CT | θ=0° | - | - | 2 | % | Note11-6 |
| Viewing Angle | θ11,θ12, θ21,θ22 | θ=30° | CR≧80 | - | - | - | Note11-1 V255 |

*1) (Gamma Value calculated by the result of V0/ V127/V255.)
*2) The measuring method of the optical characteristics is shown by the following figure.
A measurement device is TOPCON luminance meter BM - 7 (Measurement angle 1°).

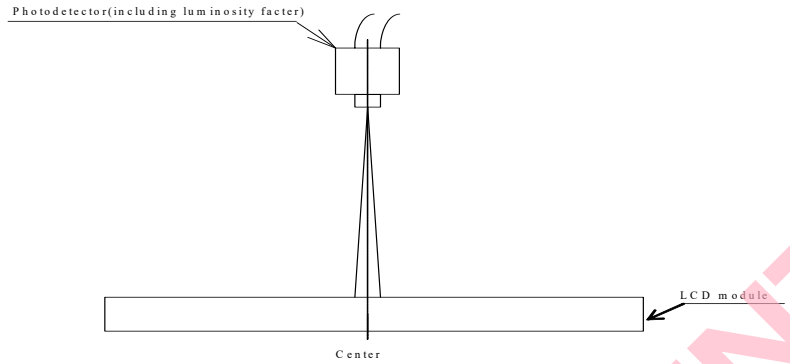



Fig. 13

Note 11-1) Contrast / NTSC / GAMMA / viewing angle is defined as follows.

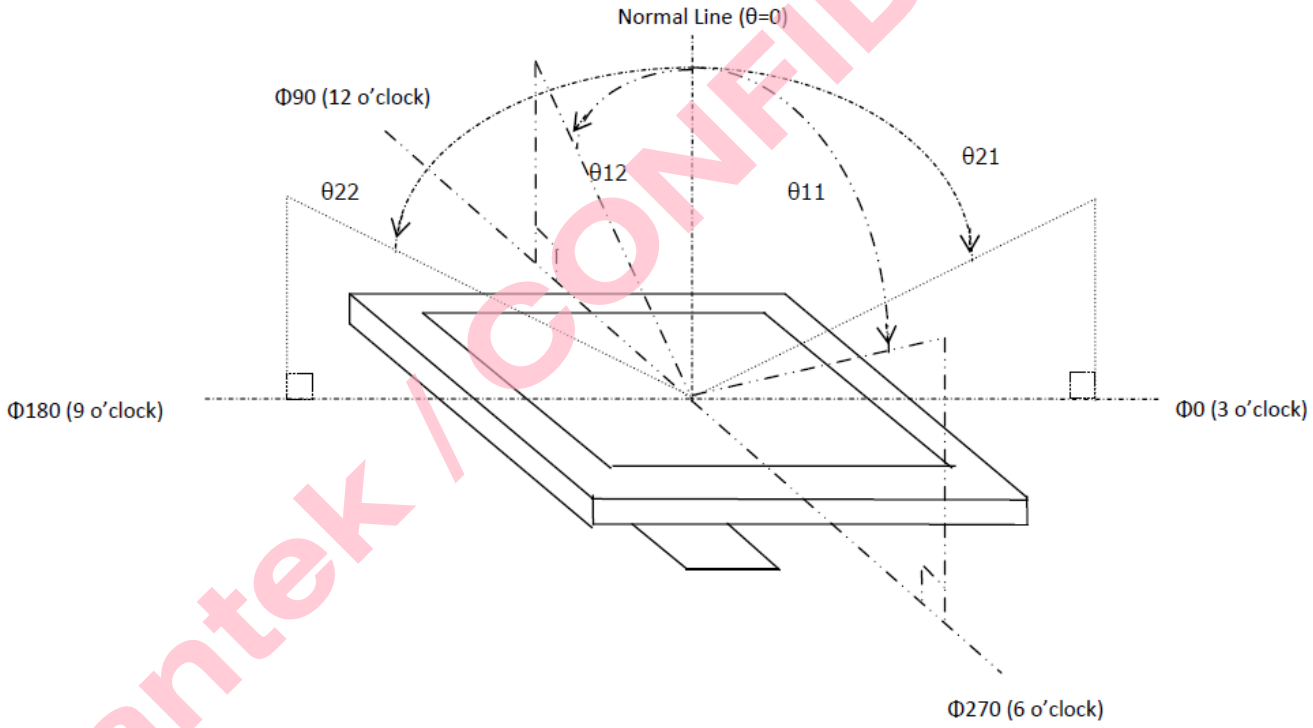



Fig. 14

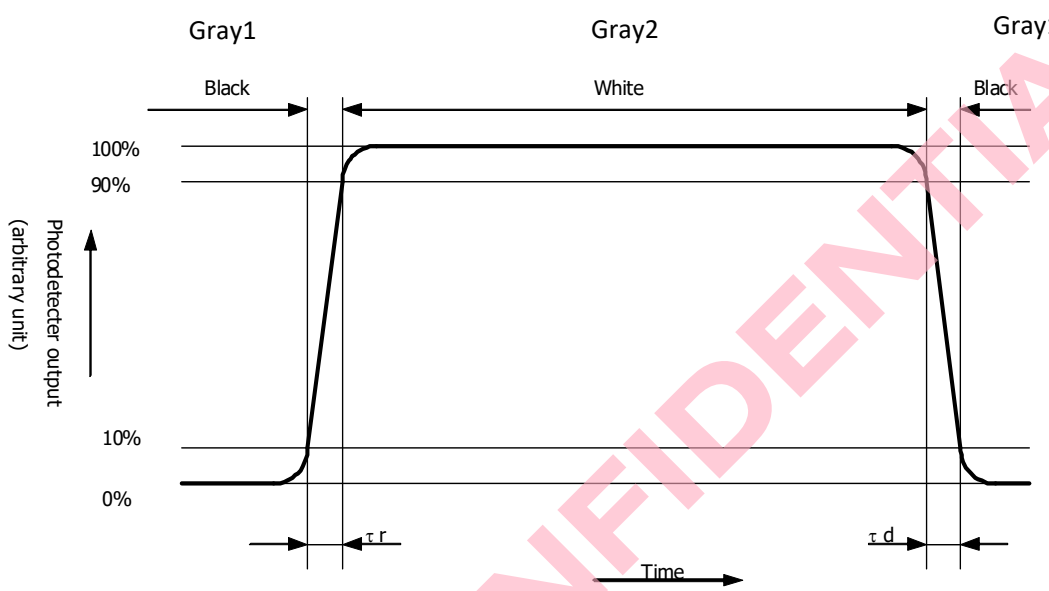
Note 11-2) Definition of contrast ratio:
The contrast ratio is defined as the follows:

$$\text{Contrast Ratio (CR)} = \frac{Luminance(brightness)\ with\ all\ pixels\ white}{Luminance(brightness) with\ all\ pixels\ black}$$

Note 11-3) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "any gray" and "any other gray"

The measured result is based LCM lighting on for 5 minutes till the temperature of panel surface is stable.




Note 11-4) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{Minimum\ Luminance\ (brightness) in\ 9\ points}{Maximum\ Luminance\ (brightness)\ in\ 9\ points}$$

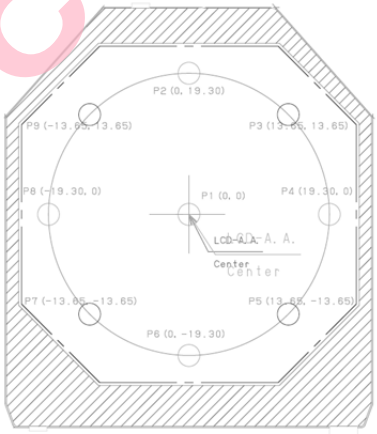


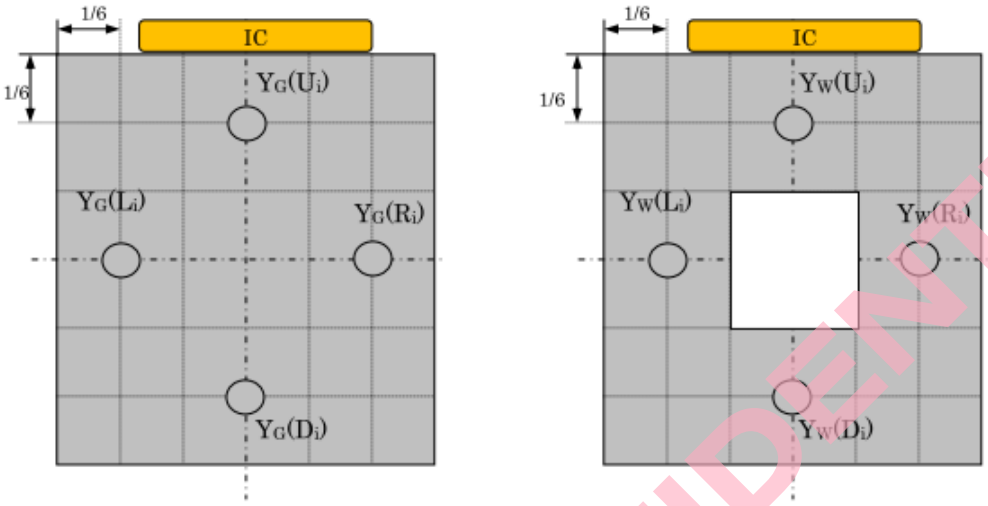
Fig. 16

Note 11-5) Measuring systems: Konica-Minolta CA-410

- Temperature = 22°C (±3°C), Frame Frequency = 72/90/120Hz, LED back-light: Duty 10%.
  Optimal VCOM adjustment for each frequency.
  Environment brightness: 150±50 lx.
- Measuring pattern : 1 column inversion.
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Flicker should measure after BL brightness became stable. Santek checked result about 4mins.
- The flicker measured condition should follow Santek related settings.

Note 11-6) Definition of Crosstalk

$CT=|Yw(Xi)-YG(Xi)|\times100(\%)/YG(Xi)$ X=U,D,L,R i=gray 127




## 10. RELIABILITY

| No. | Test item | Conditions |
|---|---|---|
| 1 | High temperature storage test | Ta = +70°C, 240h |
| 2 | Low temperature storage test | Ta = -30°C, 240h |
| 3 | High temperature operation test | Ta = +60°C, 240h |
| 4 | Low temperature operation test | Ta = -20°C, 240h |
| 5 | High temperature and high humidity operation test | Ta = +60°C90%RH, 240h |
| 6 | Thermal shock, Non-operating | Ta = -30°C (20min)～70°C(20min), 20 cycle |
| 7 | ESD test | Air Discharge: *6 corners and a center, ±6 kV, C=150pF, R=330Ω<br>Contact Discharge: *6 corners and a center, ±4 kV, C=150pF, R=330Ω |

Remark:

1.The Test samples should be applied to only one test item.

2.Sample for each test item is 2 pcs.

3.The samples must be free from defect before test, must be restored at room condition at least for 2 hours storage at room temperature after reliability test before any inspection.

4.Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

5.After a long period of high temperature,the surrounding edge of the LCM all-black image will appear MURA phenomenon,which is a normal phenomenon.

6.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

## 11. PACKING DRAWING

TBD

# 12.CAUTIONS

**a.** Recommended Storage condition: Temperature: 25ºC+/-5ºC, Humidity: ≤75%RH. Clear and free with dust and flowing particles space.
**b.** Don't disassemble and reassemble the module by yourself.
**c.** Acid, alkali, alcohol or touched directly by hand will damage the display.
**d.** Static electricity will damage the module. Please configure grounding device. And enough anti-statics protection when touching products.
**e.** The strong vibration, shock, twist or bend will cause material damage, even module broken.
**f.** It is easy to cause image sticking while displaying the same pattern for very long time.
**g.** The response time, brightness and performance will vary from different temperature.
**h.** LCD Devices are made of fragile material such as Glass and may be broken or cracked if dropped it, so please handle them with care. Please be careful not to cut your hand if you break the glass.
**i.** Do not stack the LCDs to avoid the LCDs damage and contamination.
**j.** Before using the LCDs, please check the specification.
**k.** LCDs contain a small amount of Liquid Crystal. Please follow local ordinances or regulations for disposal.
**l.** LCD shall be stored in same packing material during import, and under the condition of room temperature (20-30 degree C).
**m.** Please do not leave LCD modules under the direct sunlight or strong infra-red radiation for a long period time to prevent liquid crystal deteriorating.
**n.** Please turn off the power supply before plugging or unplugging LCD module.
**o.** Please do not rub, push, or hit LCD surface with hard tool etc. Film on surface is easily scratched, when droplets of water or dirt are on the surface, please gently remove them with soft fabric.
**p.** Handling of main and LED FPC (Flexible Printed Circuit), please be careful, do not strongly pull or scratch FPC, to avoid failure of the components and bonding part.

# 13.LIMITED WARRANTY

Unless otherwise agreed between Santek and customer, Santek will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with Santek LCD acceptance standards(copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to Santek within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Santek limited to repair and/or replacement on the terms set forth replacement on the terms setforth above. Santek shall not be responsible for any subsequent or consequential events.

## 13.1 Returning LCM Under Warranty –Terms and Conditions

**a.** No warranty can be granted if the precautions stated above have been disregarded.
The typical examples of violations are:
- Broken LCD glass.
- Circuit modified in any way, including addition of components.

**b.** Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB's eyelet, conductors and terminals.